Service Guide

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For Safety information, Warranties, and Regulatory information, see the pages at the end of the book.

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Agilent Technologies 16557D 140-MHz State/500-MHz Timing Logic Analyzer (16700-series Version)

Agilent Technologies 16557D 140-MHz State/500-MHz Timing Logic Analyzer

The Agilent Technologies 16557D is a 140-MHz State/500-MHz Timing Logic Analyzer module for the Agilent Technologies 16700-series Logic Analysis Systems. The 16557D offers high performance measurement capability.

Features

Some of the main features of the 16557D are as follows:

- 64 data channels
- 4 clock/data channels
- 2032K memory depth per channel
- 140-MHz maximum state acquisition speed
- 500-MHz maximum timing acquisition speed
- Expandable to 204 channels

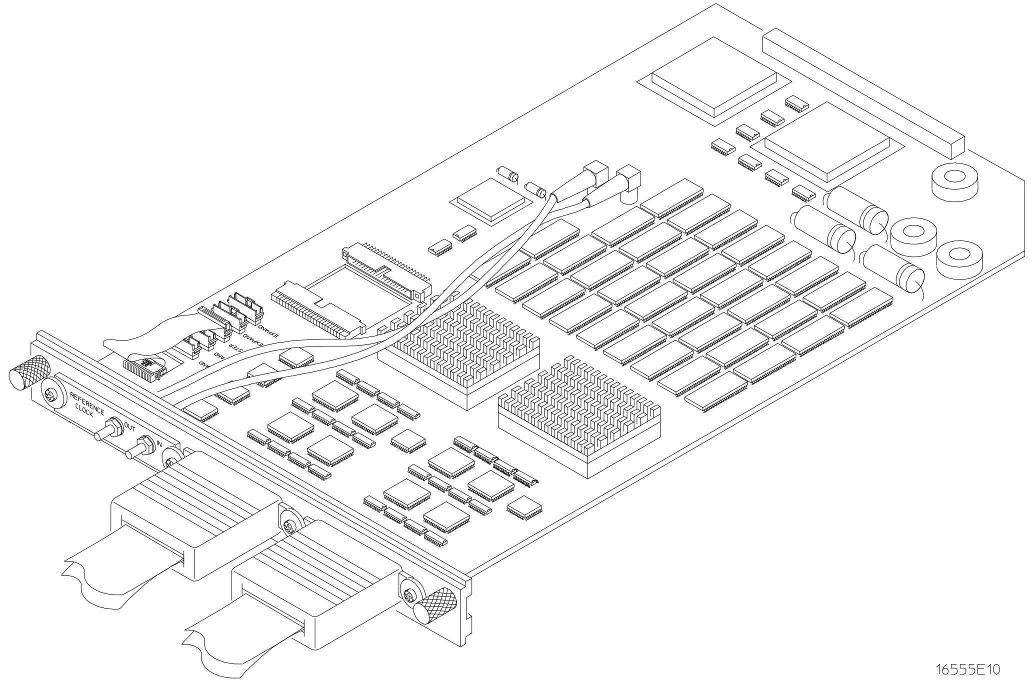
Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16557D state and timing analyzer module.

This module can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

Application

This Service Guide applies to an 16557D module installed in the Agilent Technologies 16700-series Logic Analysis System mainframes, using operating system version A.02.00 or higher. If your mainframe operating system is older than version A.02.00, contact your Agilent Technologies Service Center for newer software before attempting the performance verification procedures in chapter 3. If you are using the 16557D in an Agilent Technologies 16500C mainframe, use the 16500C version of the Agilent Technologies 16557D Service Guide.



The Agilent Technologies 16557D Logic Analyzer

In This Book

This book is the service guide for the Agilent Technologies 16557D 140-MHz State/500-MHz Timing Logic Analyzer module. Place this service guide in the 3-ring binder supplied with your Agilent Technologies 16700-series Logic Analysis System Service Manual.

This service guide is divided into eight chapters.

Chapter 1 contains information about the module and includes accessories for the module, specifications and characteristics of the module, and a list of the equipment required for servicing the module.

Chapter 2 tells how to prepare the module for use.

Chapter 3 gives instructions on how to test the performance of the module.

Chapter 4 contains calibration instructions for the module.

Chapter 5 contains self-tests and flowcharts for troubleshooting the module.

Chapter 6 tells how to replace the module and assemblies of the module and how to return them to Agilent Technologies.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the analyzer works and what the self-tests are checking.

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General Information

Accessories

The following accessories are supplied with the 16557D Logic Analyzer.

Accessories Supplied	Agilent Part Number
Probe Tip Assembly, Qty 4	01650-61608
Grabbers, Qty 4 packages	5090-4356
Extra Probe Leads, Qty 1 package	5959-9333
Extra Probe Grounds, Qty 4 packages	5959-9334
Probe Cable and Pod Labels, Qty 1	01650-94312
Double Probe Adapter, Qty 1	16542-61607

Mainframe and Operating System

The Agilent Technologies 16557D Logic Analyzer requires an Agilent Technologies 16700-series Logic Analysis System with operating system version A.01.30.00 or higher to obtain the 140-MHz state speed specification. On operating system versions prior to version A.01.30.00, the maximum state speed specification is 135 MHz.

NOTE

Earlier versions of the Agilent Technologies 16700A/01A/02A mainframe only contained two cooling fans, and might not provide adequate cooling to ensure reliable 140-MHz performance. If the first six digits of the Agilent Technologies 16700A/01A/02A serial number (located on the back of the instrument) are US3849 or higher, the instrument is a three-fan model and there is sufficient cooling.

Specifications

The specifications are the performance standards against which the product is tested.

Threshold Accuracy	± (100 mV + 3% of threshold setting)
Maximum State Speed	140 MHz *
Minimum Master-to-Master Clock Time *	7.142 ns **

Setup/Hold Time for Different Clock Schemes: *

Single Clock, Single Edge:	-0.5/3.5 ns through 3.0/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges:	-0.5/4.0 ns through 3.5/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges:	-0.5/4.5 ns through 4.0/0.0 ns, adjustable in 500-ps increments

Specified for an input signal VH = -0.9 V, VL = -1.7 V, and threshold = -1.3 V.

* 100 MHz for a five-card module.

** 10.000 ns for a five-card module.

Characteristics

The characteristics are not specifications, but are included as additional information.

	Full Channel	Half Channel *
Maximum State Clock Rate		
One, Two, Three, Four Cards	140 MHz	Not applicable
Five Cards	100 MHz	Not applicable
Maximum Conventional Timing Rate	250 MHz	500 MHz
Channel Count per Card	68	34
Channel Count per Three-Card Module	204	102
Channel Count per Five-Card Module	340	170
Memory Depth	2032K	4177K

* Half channel mode is only available for timing analysis.

Environmental Characteristics

Probes

Maximum Input Voltage	± 40 V, CAT I

Auxiliary Power

Power Through Cables	1/3 amp at 5 V maximum per cable.

Operating Environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 95% relative humidity at +40 °C (+122 °F).
Altitude	To 4600 m (15,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Operating power supplied by mainframe

Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part	Use*
Pulse Generator	140 MHz, 3.0 ns pulse width, $<$ 600 ps rise time	8133A Option 003	P, T
Digitizing Oscilloscope	$\geq$ 6 GHz bandwidth, $<$ 58 ps rise time	54750A mainframe with 54751A plug-in module	P
Function Generator	Accuracy $\leq (5)(10^{-6}) \times$ frequency, DC offset voltage ± 1.5 V	3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A	P
BNC-Banana Cable		11001-60001	P
BNC Tee	BNC (m)(f)(f)	1250-0781	P
Cable	BNC (m-m) 48 inch	10503A	P
SMA Coax Cable (Qty 3)	$\geq$ 18 GHz bandwidth	8120-4948	P
BNC Coax Cable	BNC (m-m), $>$ 2 GHz bandwidth	8120-1840	P
Adapter (Qty 4)	SMA(m)-BNC(f)	1250-1200	P
Adapter	SMA(f)-BNC(m)	1250-2015	P
Coupler	BNC (m-m)	1250-0216	P
20:1 Probes (Qty 2)		54006A	P
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P, T

A = Adjustment, P = Performance Tests, T = Troubleshooting

**Instructions for making these test connectors are in chapter 3, “Testing Performance.”

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Preparing for Use

Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed in chapter 1. Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the module within the following ranges:

Temperature: +20 °C to +35 °C (+68 °F to +95 °F)

Humidity: 20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to +75 °C (-40 °F to +167 °F)
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

Accessories supplied with the module are listed in chapter 1, “Accessories” on page 10.

3 Inspect the product for physical damage.

Check the module and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To prepare the mainframe

CAUTION Turn off the mainframe power before removing, replacing, or installing the module.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1 Remove power from the instrument.

a Exit all logic analysis sessions. In the session manager, select Shutdown.
b At the query, select Power Down.
c When the “OK to power down” message appears, turn the instrument off.
d Disconnect the power cord.
e Disconnect any input or output connections.

2 Plan your module configuration.

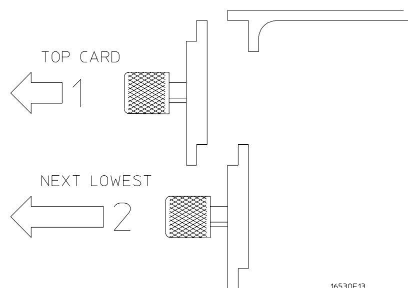
If you are installing a one-card module, use any available slot in the mainframe.

If you are installing a multi-card module, use adjacent slots in the mainframe.

3 Loosen the thumb screws.

Cards or filler panels below the slots intended for installation do not have to be removed.

Starting from the top, loosen the thumb screws on filler panels and cards that need to be moved.



4 Starting from the top, pull the cards and filler panels that need to be moved halfway out.

CAUTION All multicard modules will be cabled together. Pull these cards out together.

5 Remove the cards and filler panels.

Remove the cards or filler panels that are in the slots intended for the module installation. Push all other cards into the card cage, but not completely in. This is to get them out of the way for installing the module.

Some modules for the Logic Analysis System require calibration if you move them to a different slot. For calibration information, refer to the manuals for the individual modules.

To configure a one-card module

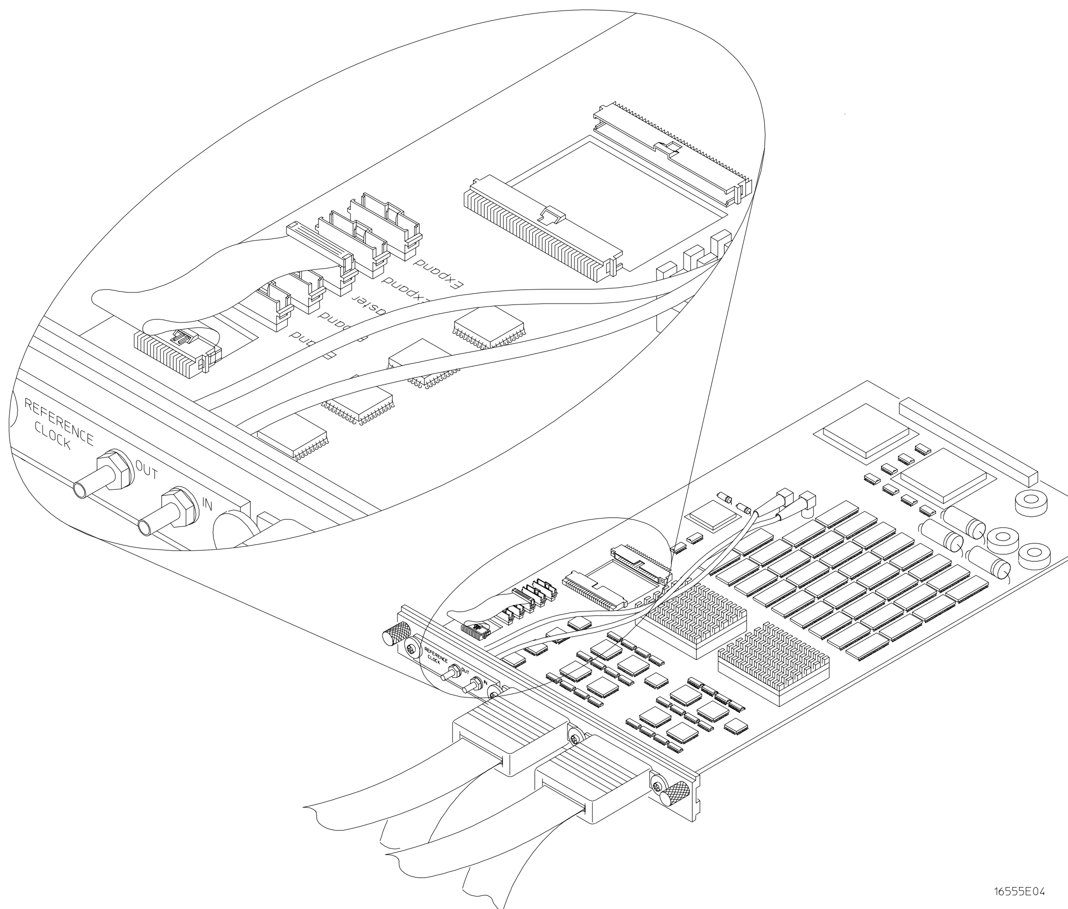
- When shipped separately, the module is configured as a one-card module. The cables should be connected as shown in the figure.
- To configure a multicard module into one-card modules, remove the cables connecting the cards. Then connect the free end of the 2x10 cable to the connector labeled "Master" (J6) on each card (see figure below).

CAUTION

If you pull on the flexible ribbon part of the 2x10 cable, you might damage the cable assembly. Using your thumb and finger, grasp the ends of the cable connector. Apply pressure to the ends of the cable connector to disengage the metal locking tabs of the connector from the cable socket on the board. Then pull the connector from the cable socket.

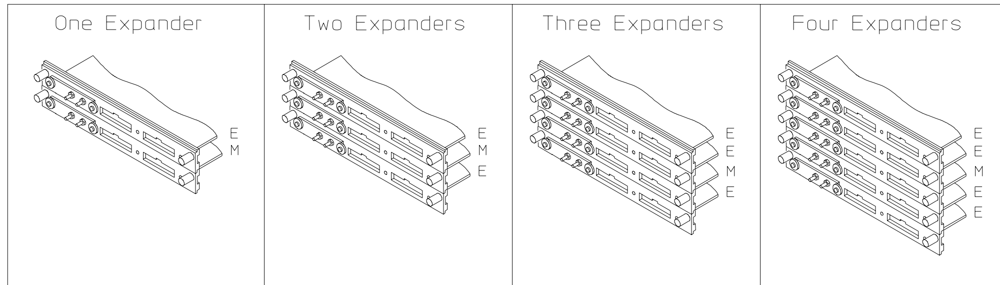
NOTE

Save unused cables for future configurations.

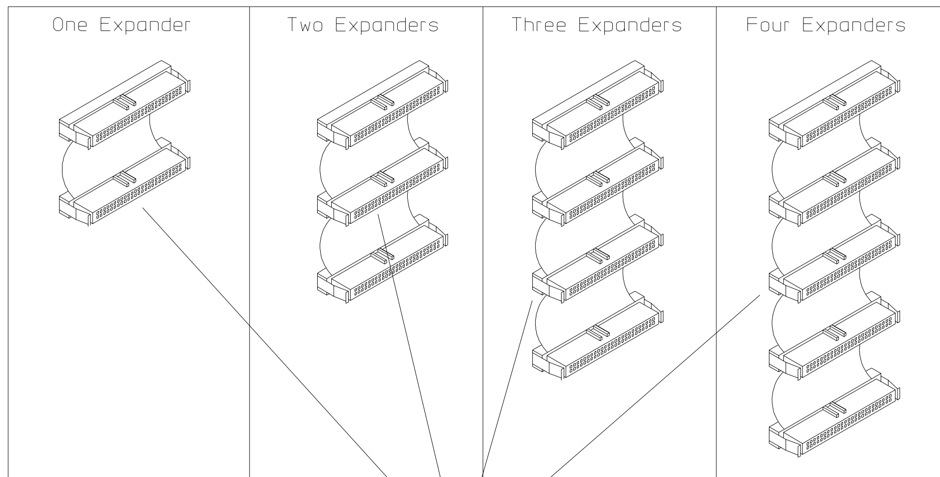


To configure a multi-card module

1 Plan the configuration. Multicard modules can only be connected as shown in the illustration. Select the card that will be the master card, and set the remaining cards aside.

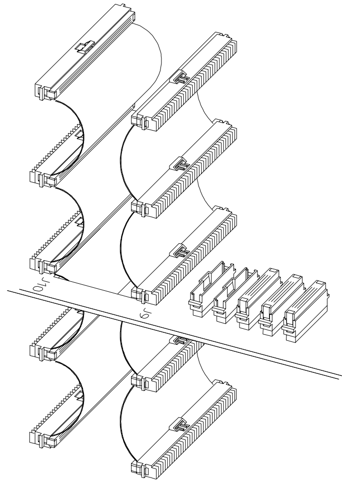


2 Obtain two 2x25 cables from the accessory pouch that match the number of expander cards being configured. The illustration shows the cables that are available and which cable is used in each expander configuration.



This connector is plugged into the Master Card.

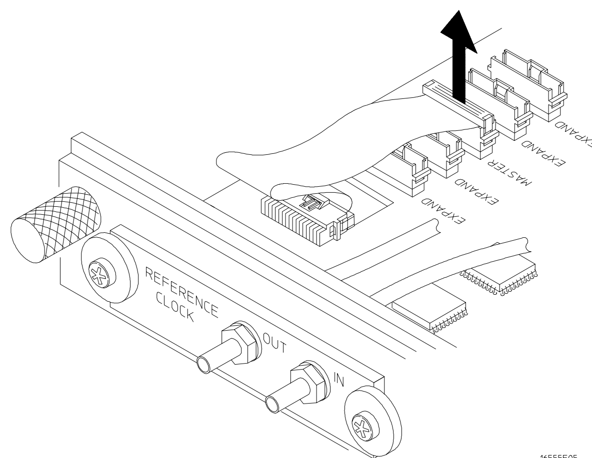
3 Look at the illustration in the previous step. The illustration shows which of the cable connectors is plugged into the master card. Plug one 2x25 cable into the master card J9. Observe which cable connector (as shown in the illustration) is plugged into J9. Follow the same procedure to connect the second 2x25 cable into the master card J10. Cable connectors are keyed; do not force.



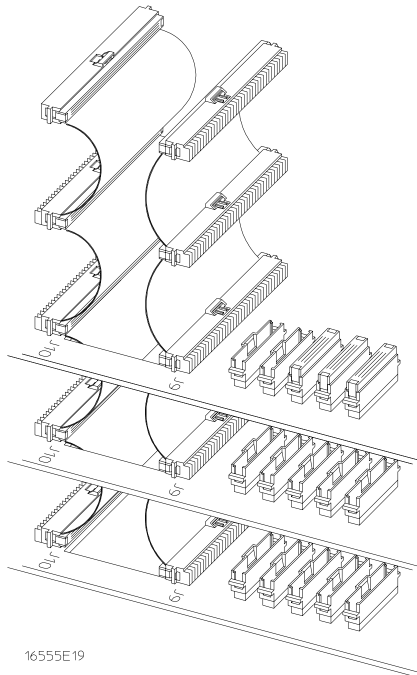
4 On the expander cards, disconnect the end of the 2x10 cable that is plugged into the connector labeled "Master."

CAUTION

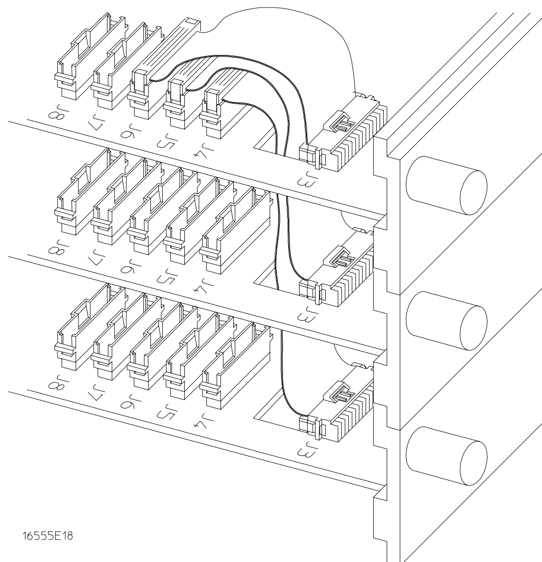
If you pull on the flexible ribbon part of the 2x10 cable, you might damage the cable assembly. Using your thumb and finger, grasp the ends of the cable connector. Apply pressure to the ends of the cable connector to disengage the metal locking tabs of the connector from the cable socket on the board. Then pull the connector from the cable socket.



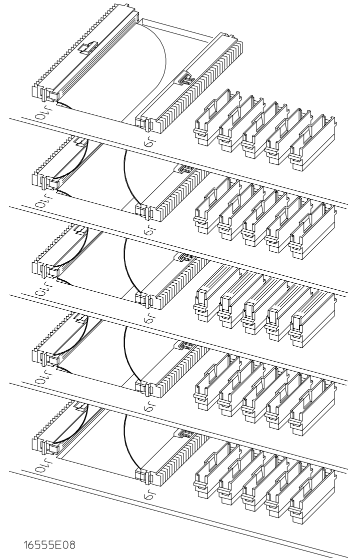
5 Place the master card on top of any expander cards that go under the master card. Feed the 2x25 cables that are plugged into the master card through the cable access holes of the expander cards. Plug the 2x25 cables into J9 and J10 of the expander cards.



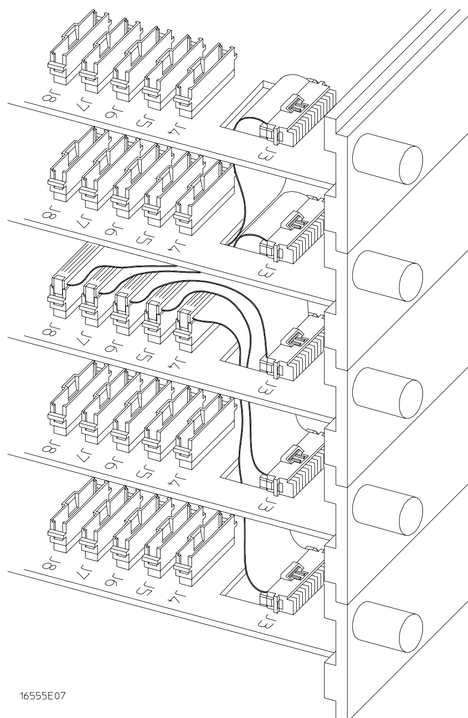
6 Feed the free end of the 2x10 cables of the expander cards through the access holes to the master card. Plug the 2x10 cables into J4 (bottom-most expander in a five-card configuration) and J5 (expander that is next to the master card) on the master card.



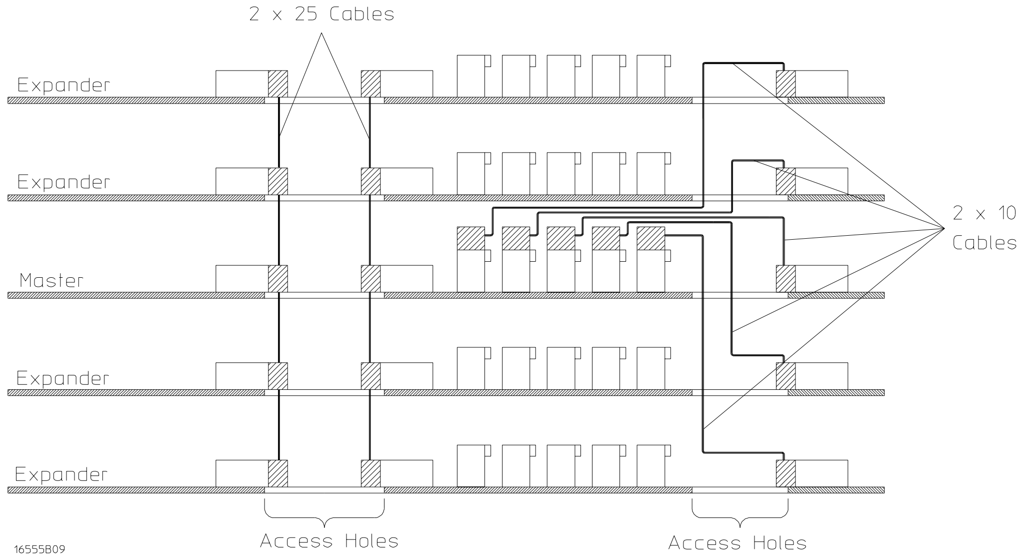
7 Place the remaining expander boards on top of the master board. Feed the 2x25 cables that are plugged into the master card through the cable access holes of the expander cards. Plug the 2x25 cables into J9 and J10 of the expander cards.



8 Feed the free end of the 2x10 cables of the expander cards through the access holes to the master card. Plug the 2x10 cables into J7 (expander that is next to the master card) and J8 (top-most expander in a four- or five-card configuration) on the master card.



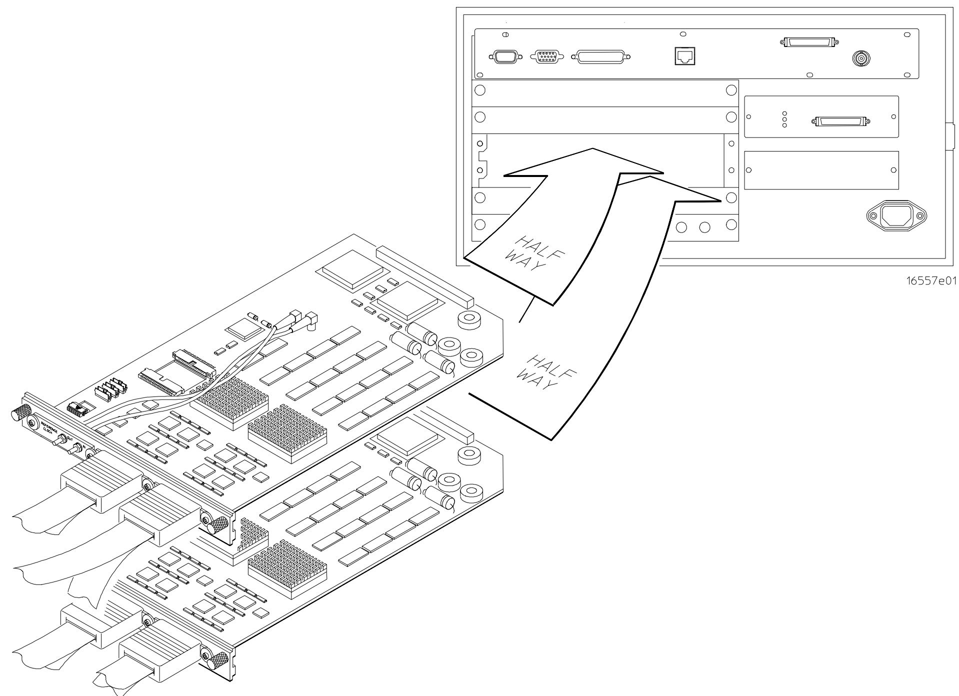
9 The following illustration shows the proper connection of the 2x25 cables and the 2x10 cables for a five-card module. If a two-, three-, or four-card module is configured, not all cables will be present; however, the existing cables will be routed in the same manner. Make sure ALL cables are firmly seated.



To install the module

1 Slide the cards above the slots for the module about halfway out of the mainframe.

2 With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



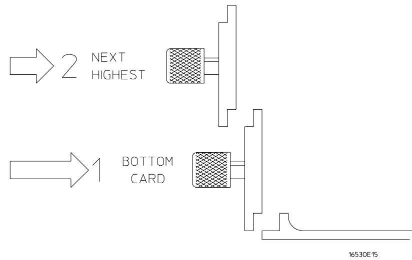
3 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 5.

4 Position all cards and filler panels so that the endplates overlap.

5 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.



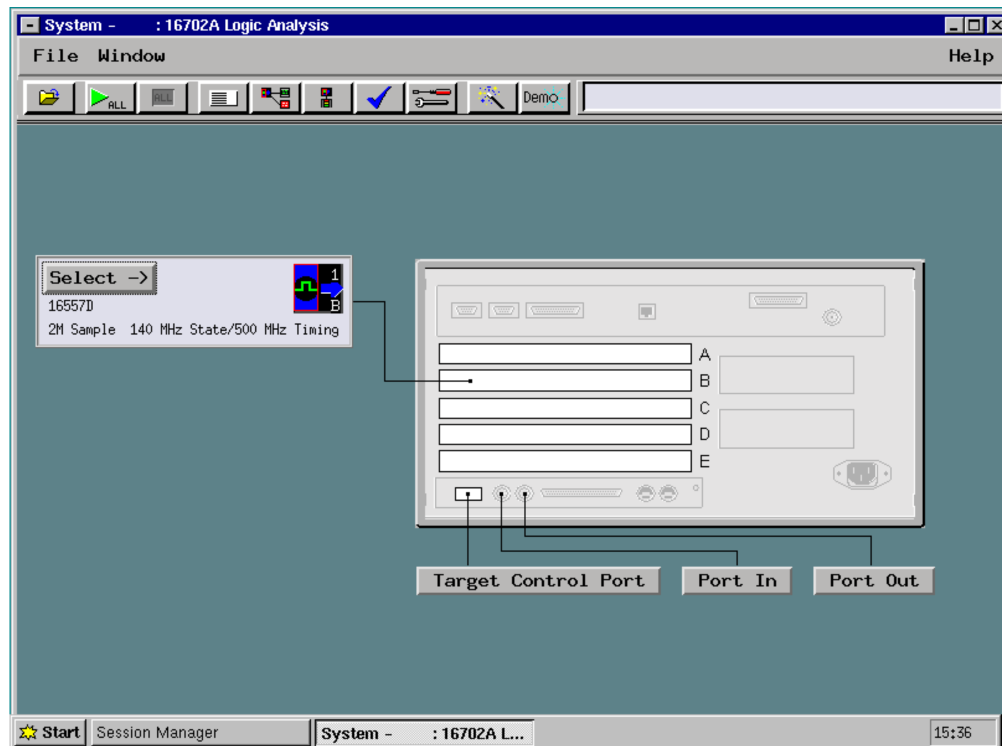
CAUTION Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To turn on the system

1 Connect the power cable to the mainframe.

2 Turn on the instrument power switch.

When you turn on the instrument power switch, the instrument performs powerup tests that check mainframe circuitry. After the powerup tests are complete, the screen will look similar to the sample screen below.



To test the module

The logic analyzer module does not require an operational accuracy calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the module does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

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Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, software tests (self-tests) and manual performance tests are done. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a “Pass” status for each of the tests.

Test Strategy

This chapter shows the module being tested in an Agilent Technologies 16700B-series mainframe.
For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test.

One-card Module. To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Multi-card Module. To perform a complete test on a multi-card module, perform the self-tests with the cards connected. Then, remove the multi-card module from the mainframe and configure each card as a one-card module. Install the one-card modules into the mainframe and perform the one-card manual performance verification tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into a multi-card module, reinstall it into the mainframe and perform the final multi-card test. For removal instructions, see Chapter 6, “Replacing Assemblies.” For installation and configuration instructions, see Chapter 2, “Preparing for Use.”

Test Interval

Test the performance of the module against specifications at two-year intervals.

Test Record Description

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the module over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the instrument and the test equipment for 30 minutes.

To Perform the Self-tests

There are two types of self-tests: self-tests that automatically run at power-up, and self-tests that you select on the screen. The self-tests verify the correct operation of the logic analysis system. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

Perform the power-up tests

The logic analysis system automatically performs power-up tests when you apply power to the instrument. Any errors are reported in the boot dialogue. Serious errors will interrupt the boot process.

The power-up tests are designed to complement the instrument on-line Self Tests. Tests that are performed during power-up are not repeated in the Self Tests.

The monitor, keyboard and mouse must be connected to the mainframe to observe the results of the power-up tests.

1. **Disconnect all inputs and exit all logic analysis sessions.**

   In the Session Manager, select **Shutdown**. In the window, select **Powerdown**.

2. **When the “OK to power down” message appears, turn off the power switch.**
3. **After a few seconds, turn the power switch back on. Observe the boot dialogue for the following:**

   - ensure all of the installed memory is recognized
   - any error messages
   - interrupt of the boot process with or without error message

   A complete transcript of the boot dialogue is in the Agilent Technologies 16700-series *Logic Analysis System Service Guide*, Chapter 8, “Theory of Operation”.

4. **During initialization, check for any failures.**

   If an error or an interrupt occurs, refer to the Agilent Technologies 16700-series *Logic Analysis System Service Guide*, Chapter 5, “Troubleshooting”.

Perform the self-tests

The self-tests verify the correct operation of the logic analysis system and the installed 16557D module. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analysis system, run the self-tests all at once.

1 Launch the Self-Tests.

a In the System window, click on System Admin.

b Under the Admin tab, click on Self-Test . . .

c In the query pop-up, select Yes to exit the current session.

The Self-Test closes down the current session because the test algorithms leave the system in an unknown state. Re-launching a session at the end of the tests will ensure the system is properly initialized.

2 In the Self-Test window select Test All.

When the tests are finished, the Status will change to TEST passed or TEST failed. You can find detailed information about the test results in the Status Message field of the Self-Test window.

The System CPU Board test returns Untested because the CPU tests require user action. To test the CPU Board, select CPU Board, then select each test individually.

3 Select Quit to exit the Test menu.

4 In the Session Manager, select Start Session This Display to re-launch a logic analysis session.

To Make the Test Connectors

The test connectors connect the logic analysis system to the test equipment.

Materials Required

Description	Recommended Agilent Part	Qty
BNC (f) Connector	1250-1032	4
100 Ω 1% resistor	0698-7212	6
Berg Strip. 17-by-2		1
Berg Strip, 6-by-2		3
20:1 Probe	54006A	2
Jumper wire		

1 **Build three test connectors using BNC connectors and 6-by-2 sections of Berg strip.**

a Solder a jumper wire to all pins on one side of the Berg strip.

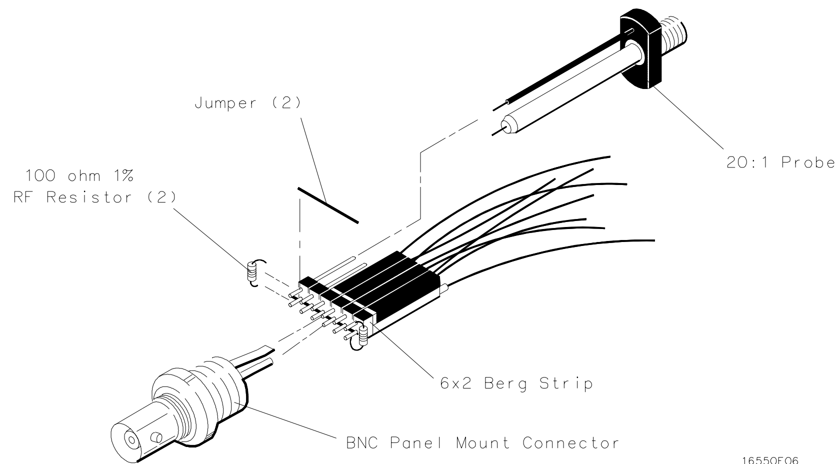
b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder two resistors to the Berg strip, one at each end between the end pins.

d Solder the center of the BNC connector to the center pin of one row on the Berg strip.

e Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.

f On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



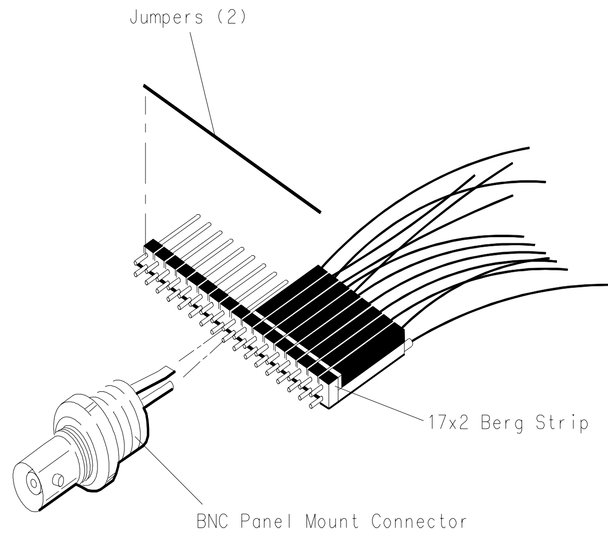
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



To Set up the Test Equipment and the Analyzer

Before testing the specifications of the 16557D logic analyzer, the test equipment and the logic analysis system must be set up and configured.

These instructions include detailed steps for initially setting up the required test equipment and the logic analysis system. Before performing any or all of the following tests in this chapter, the following steps must be followed.

NOTE Multi-card modules must be separated into single-card modules.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/ Part
Pulse Generator	140 Mhz, 3.0 ns pulse width, $<$600 ps rise time	8133A option 003
Digitizing Oscilloscope	$\geq$ 6 GHz bandwidth, $<$ 58 ps rise time	54750A w/ 54751A
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	DC offset voltage $\pm$1.5 V	3325B Option 002

Set up the equipment

1 Turn on the required test equipment listed in the table above. Let them warm up for 30 minutes before beginning any test.

2 Turn on the logic analysis system.

a Connect the keyboard, mouse, and monitor to the rear panel of the logic analysis system mainframe (16700B only).

b Plug in the power cord to the power connector on the rear panel of the mainframe.

c Turn on the main power switch on the mainframe front panel.

3 Set up the logic analysis system.

a Open the Session Manager window and select “Start Session”.

b In the Logic Analysis System window, select the module icon, then select Setup. A Setup window opens.

c In the Setup window, select Window, then select Slot n: Analyzer<n> (where “n” is the slot the module under test is installed), then select Listing. A Listing window opens.

d In the Analyzer<n> Setup window, select the Sampling tab.

4 Set up the pulse generator according to the following table.

Timebase	Channel 2	Trigger	Channel 1
Mode: Int Period: 7.142 ns	Mode: Pulse Divide: Pulse ÷ 2 Width: 3.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 2 Ampl: 0.50 V Offs: 0.00 V	Mode: Square Delay: 0.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)

5 Set up the oscilloscope.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	Display	Trigger	[Shift] Δ Time
Averaging: On # of averages: 16	Graticule graphs: 2	Level: 0.0 mV	Stop src: channel 2 [Enter]

Channel 1	Channel 2	Define meas
External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	Thresholds: user-defined Units: Volts Upper: - 980 mV Middle: -1.30 V Lower: -1.62 V

Allow the logic analysis system to warm up for 30 minutes before beginning any of the following tests.

To Test the Threshold Accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy

These instructions include detailed steps for testing the threshold settings of Pod 1. After testing Pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for Pod 1, substituting the next pod for Pod 1 in the instructions.

Equipment Required

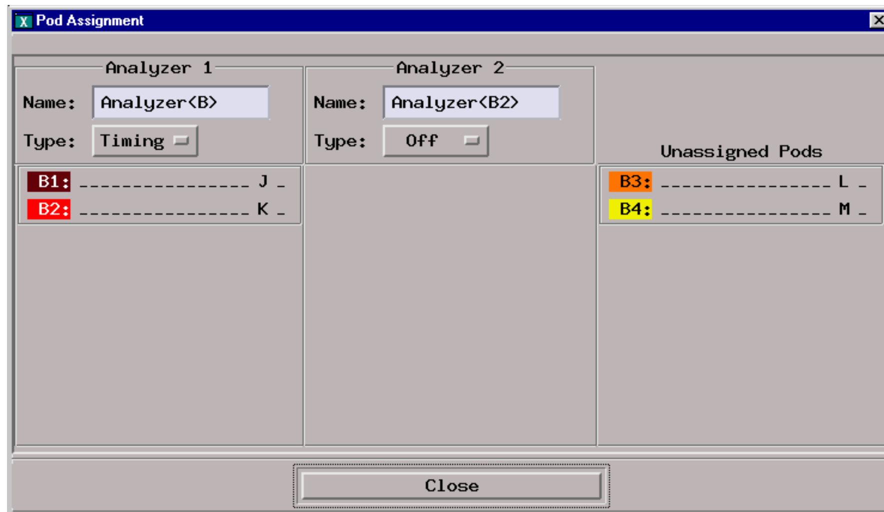
Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	DC offset voltage ±1.5 V	3325B Option 002
BNC-Banana Cable		11001-60001
BNC Tee		1250-0781
BNC Cable		8120-1840
BNC Test Connector, 17x2		

Set up the equipment

1. **If you have not already done so, perform the procedure described in “To Set up the Test Equipment and the Analyzer” on page 35.**
2. **Set up the function generator.**
   - **a** Set up the function generator to provide a DC offset voltage at the Main Signal output.
   - **b** Disable any AC voltage to the function generator output, and enable the high voltage output.
   - **c** Monitor the function generator DC output voltage with the multimeter.

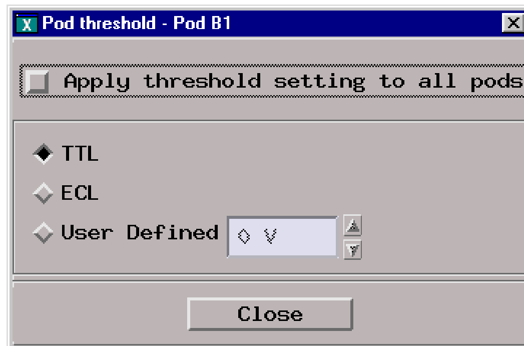
Set up the logic analyzer

1. In the Analyzer Setup window, select the Format tab.
2. Under the Format tab, select Pod Assignment. Unassign the pods that are assigned to Analyzer 2. To unassign the pods, use the mouse to drag the pods to the Unassigned Pods column.



Select Close to close the Pod Assignment window.

3. Select the Format tab, then select the Threshold field under Pod 1. Click on the checkbox next to Apply Threshold Setting to all pods to deselect.

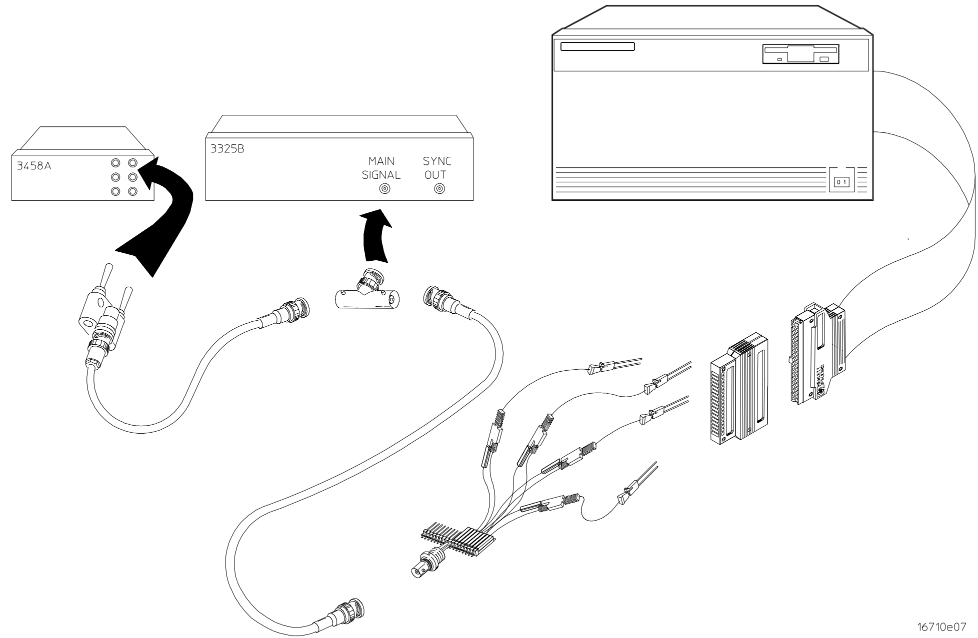


Connect the logic analyzer

1 Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of Pod 1 to one side of the BNC Tee.

2 Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.

3 Connect the BNC Tee to the Main Signal output of the function generator.

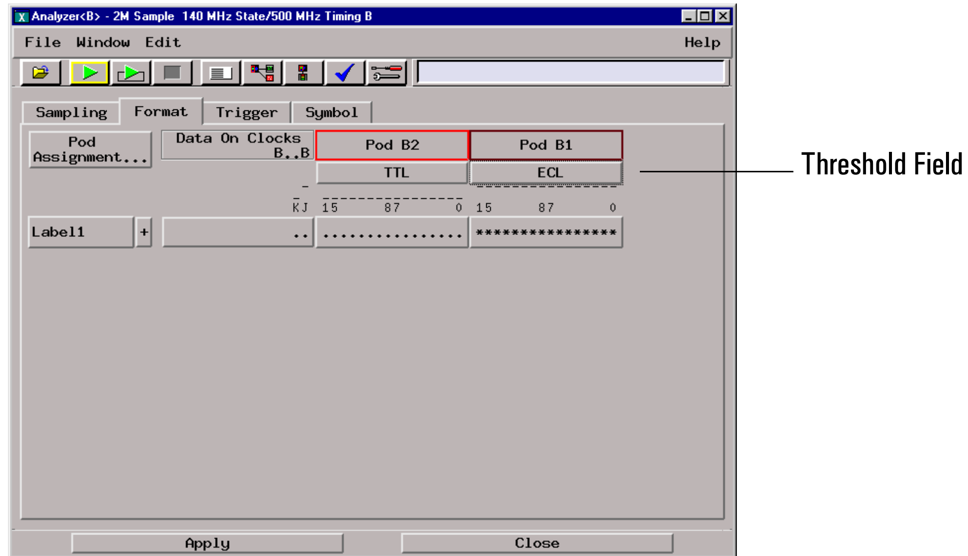


Test the ECL threshold

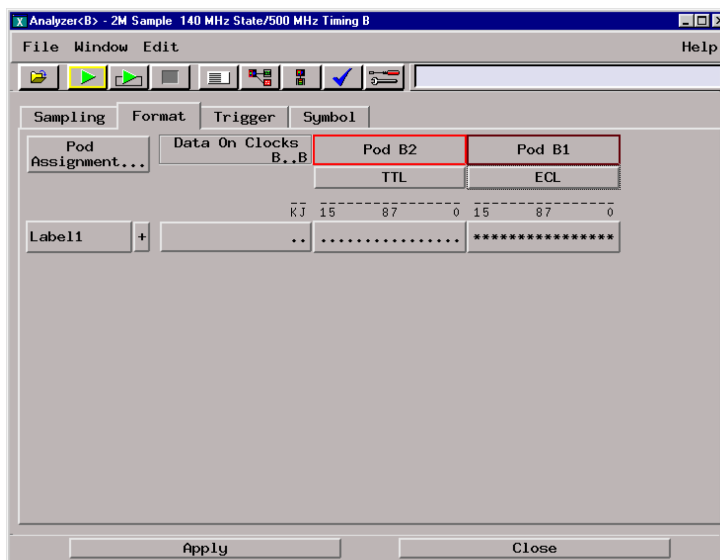
1 Under the Format tab, select the threshold field for the pod under test, then select ECL.

2 On the function generator front panel, enter -1.159 V ±1 mV DC offset. Use the multimeter to verify the voltage.

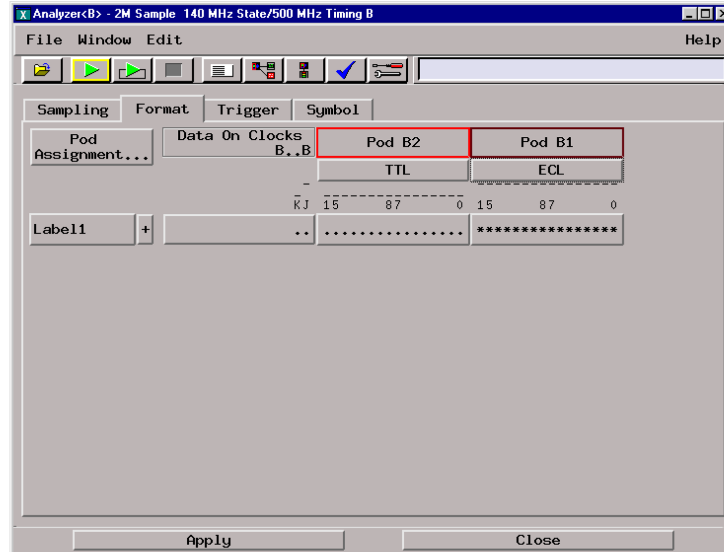
The activity indicators for Pod 1 should show all data channels and the J-clock channel at a logic high.



3 Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels are at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels are at a logic high. Record the function generator voltage in the performance test record.



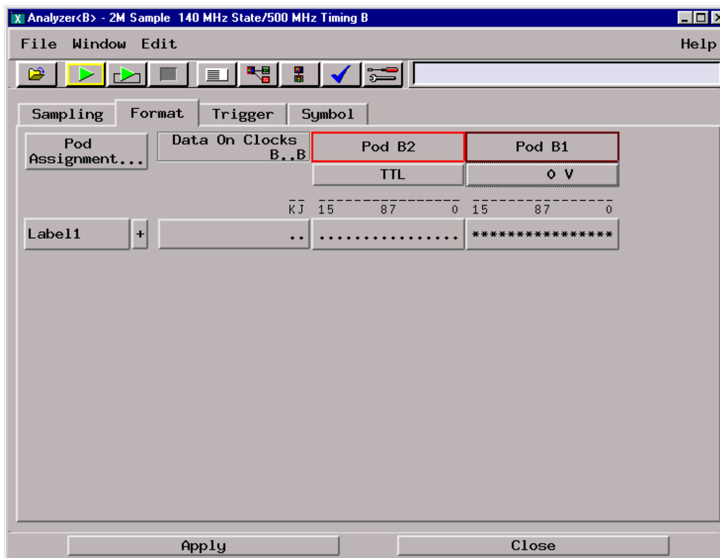
Test the 0 V User threshold

1 Under the Format tab, select the threshold field, then select User. In the numeric field, enter 0 V.

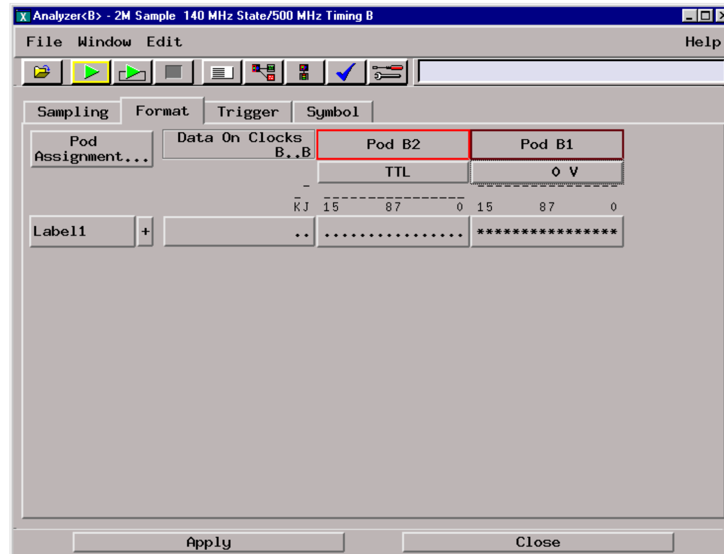
2 On the function generator front panel, enter +0.102 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for the pod under test should show all data channels and the J-clock channel at a logic high.

3 Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for the pod under test show the channels at a logic high. Record the function generator voltage in the performance test record.



Test the next pod

Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator as shown in “Connect the logic analyzer” on page 39. If you have just finished testing Pod 1, connect the data and clock channels of Pod 2. Repeat until all pods have been tested.

Note that the pod under test must be assigned to the analyzer. For Pod 3, use the Pod Assignment window under the Format tab, unassign Pods 1 and 2 and assign Pods 3 and 4 to Analyzer 1.

When you have finished testing the last pod, you have completed the threshold accuracy test.

To Test the Single-clock, Single-edge, State Acquisition

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

This test checks a combination of data channels using a single-edge clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Pulse Generator	140 Mhz, 3.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC (m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 35. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

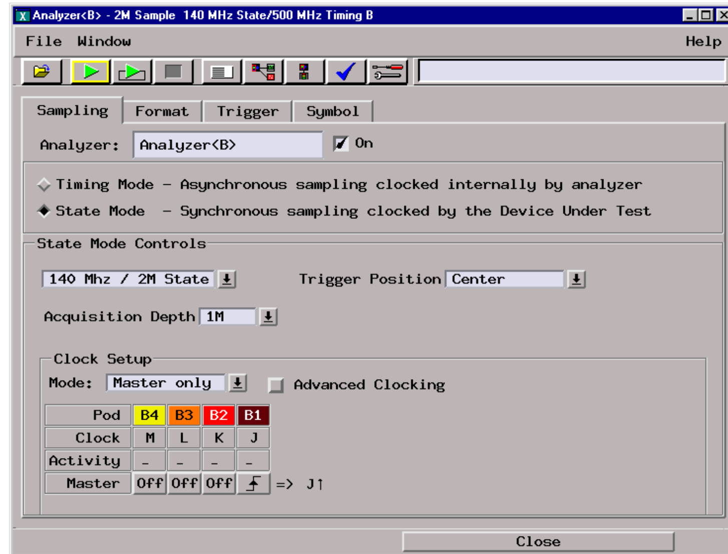
Set up the logic analyzer

1 Set up the Sampling tab.

a In the Analyzer setup window, select the Sampling tab.

b Select State mode.

c Select the 135MHz/2M state mode field, then select 140MHz/2M state.

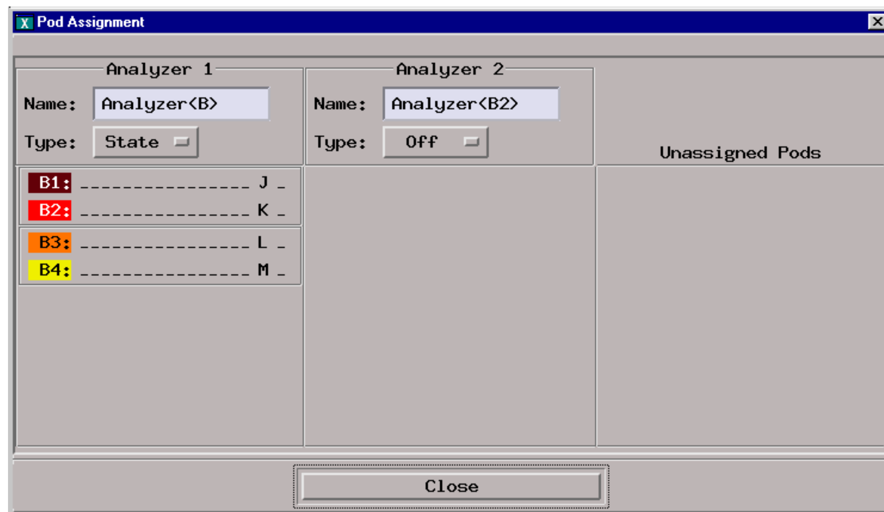


2 Assign all pods to Analyzer 1.

a In the Analyzer setup window, select Format tab.

b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods to the Analyzer 1 column.



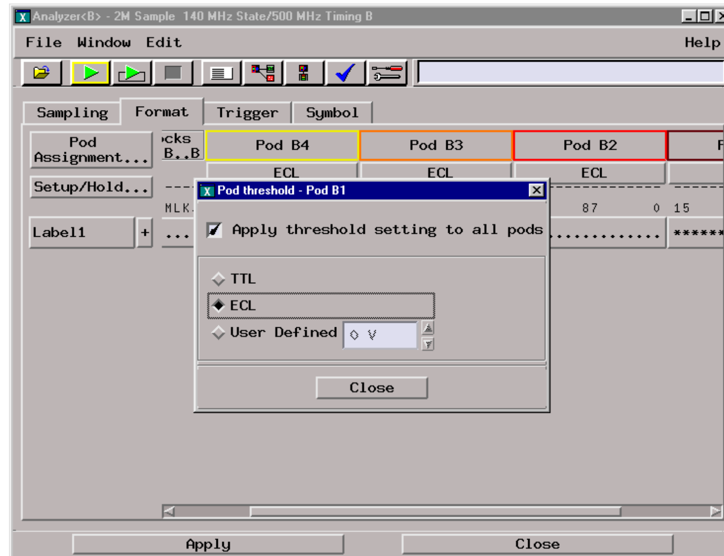
d Select Close to close the Pod Assignment window.

3 Set up the Format tab.

a Under one of the pod fields, select TTL.

b In the Pod Threshold window, ensure the Apply threshold setting to all pods checkbox is checked.

c In the Pod Threshold window, select ECL.



d Select Close to close the Pod Threshold window.

4 Set up the Trigger tab.

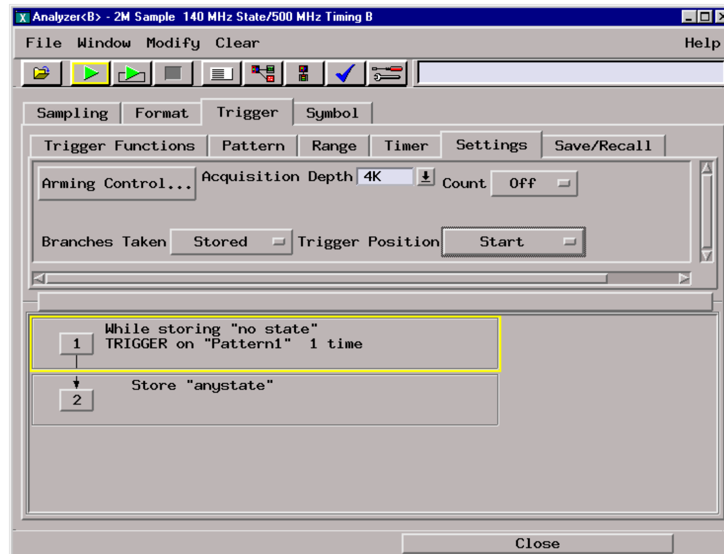
a In the Analyzer setup window, select the Trigger tab. Under the Trigger tab, select the Settings tab.

b Select the Acquisition Depth field, then select “4K”.

c Select the Count field, then select “Off”.

d Select the Trigger Position field, then select Start.

e Select the field labeled “1” in the Sequence field, then at the pop-up menu, select Edit. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.



5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window appears.

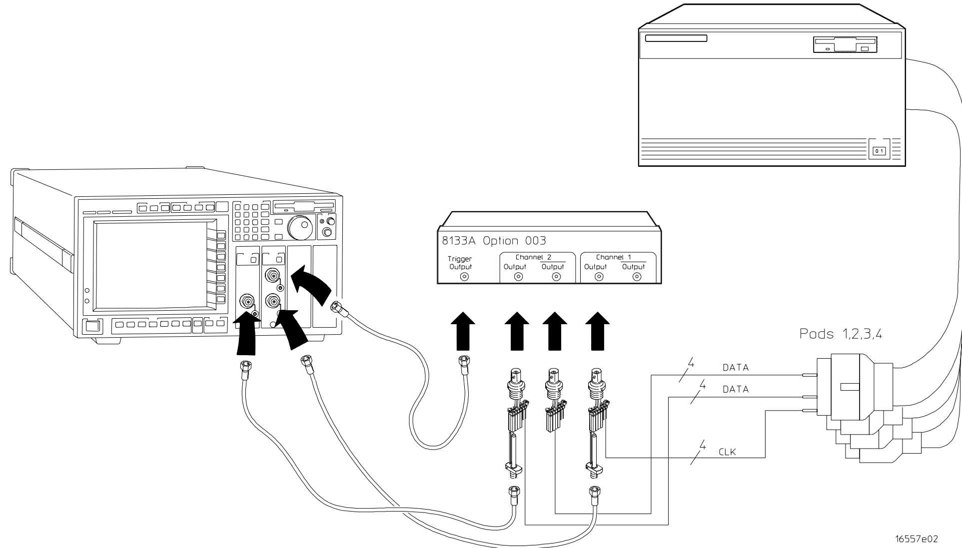
c Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

Note: Leave the Marker Setup window open. You will be entering numeric values in the “occurs” field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration.



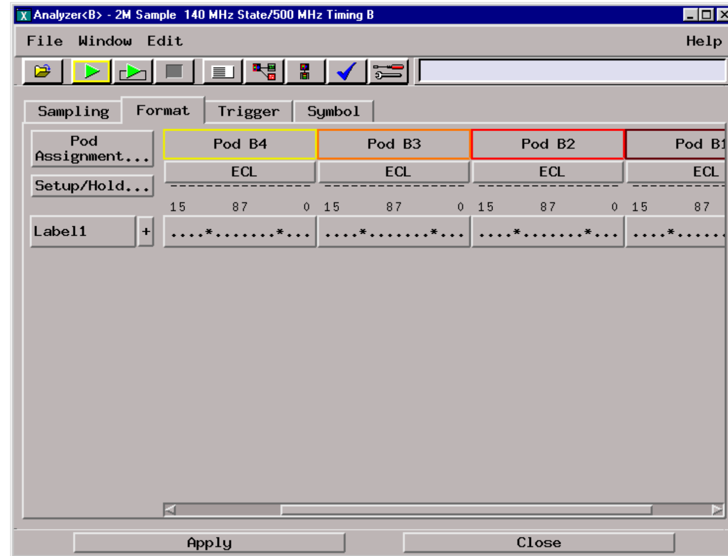
Connect the 16557D to the Pulse Generator

Agilent 8133A Ch2 Output	8133A Ch2 $\overline{\text{Output}}$	8133A Ch1 Output
Pod 1 channel 3	Pod 1 channel 11	J-clock
Pod 2 channel 3	Pod 2 channel 11	
Pod 3 channel 3	Pod 3 channel 11	
Pod 4 channel 3	Pod 4 channel 11	

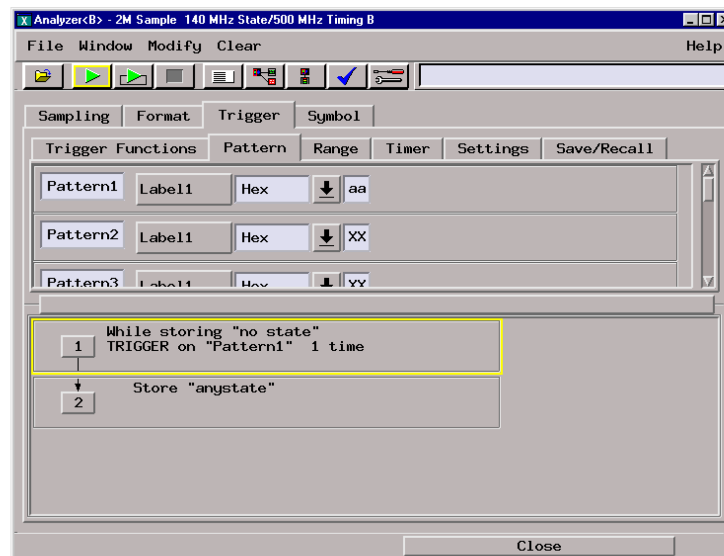
3 Activate the data channels that are connected according to the previous table.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select the data channels to be tested (channels 11 and 3 of each pod). An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



c Under the Trigger tab, select the Pattern tab. Under the Pattern tab, select the pattern field associated with pattern recognizer “Pattern 1”. Enter “aa”.



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 7.142 ns, +0 ps or -142 ps.

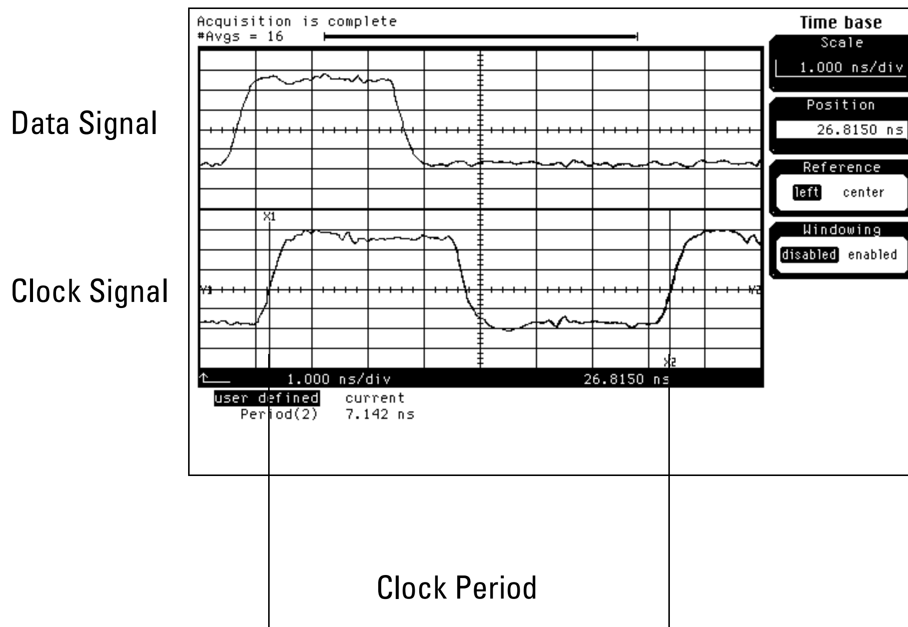
a Turn on the pulse generator channel 1, channel 2, and trigger outputs.

b In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

d On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 7.142 ns, go to step e. If the period is less than or equal to 7.142 ns but greater than 7.000 ns, go to step 2.

e In the oscilloscope Timebase menu, increase Position 7.142 ns. If the period is more than 7.142 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than or equal to 7.142 ns but greater than 7.000 ns.



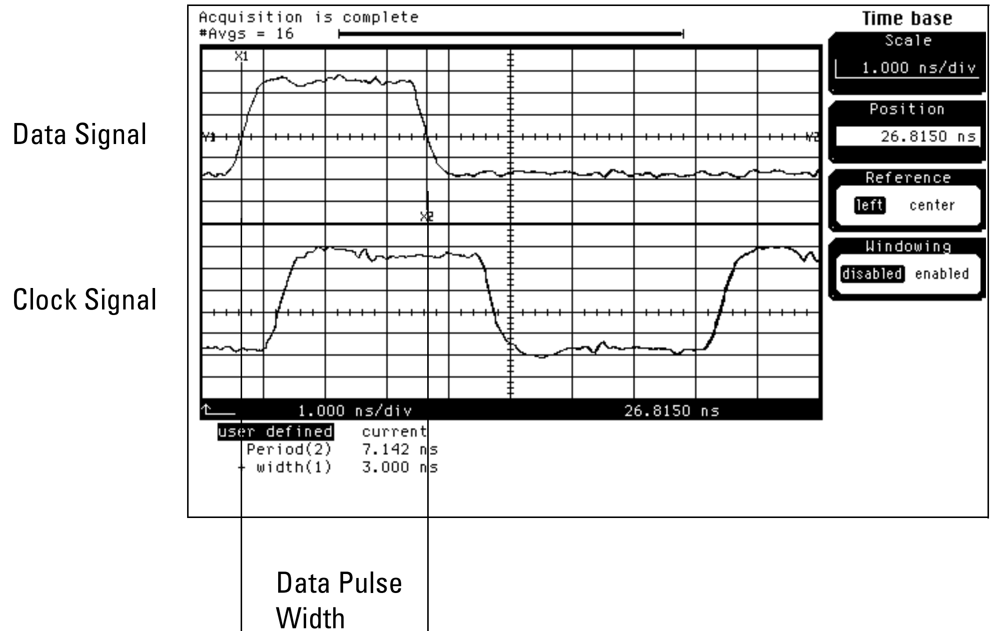
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.000 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold combination

1 Select the logic analyzer setup/hold time.

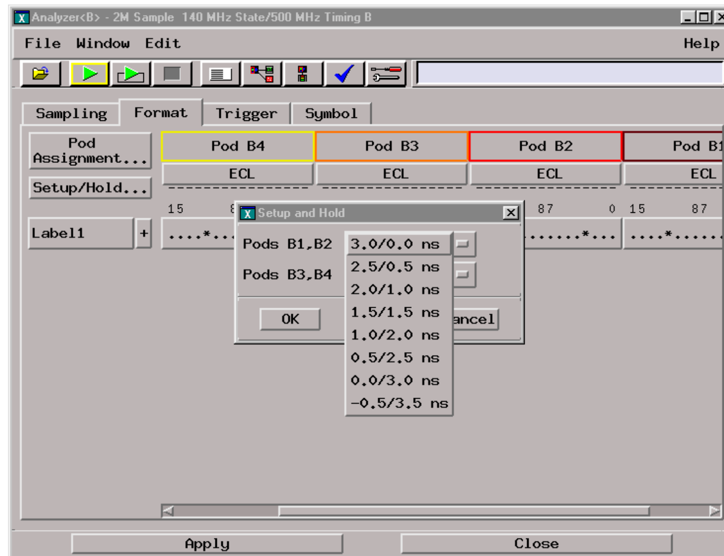
  a In the Analyzer setup window, select the Format tab.

  b Under the Format tab, select Setup/Hold.

  c In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations

3.0/0.0 ns
-0.5/3.5 ns



  d Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

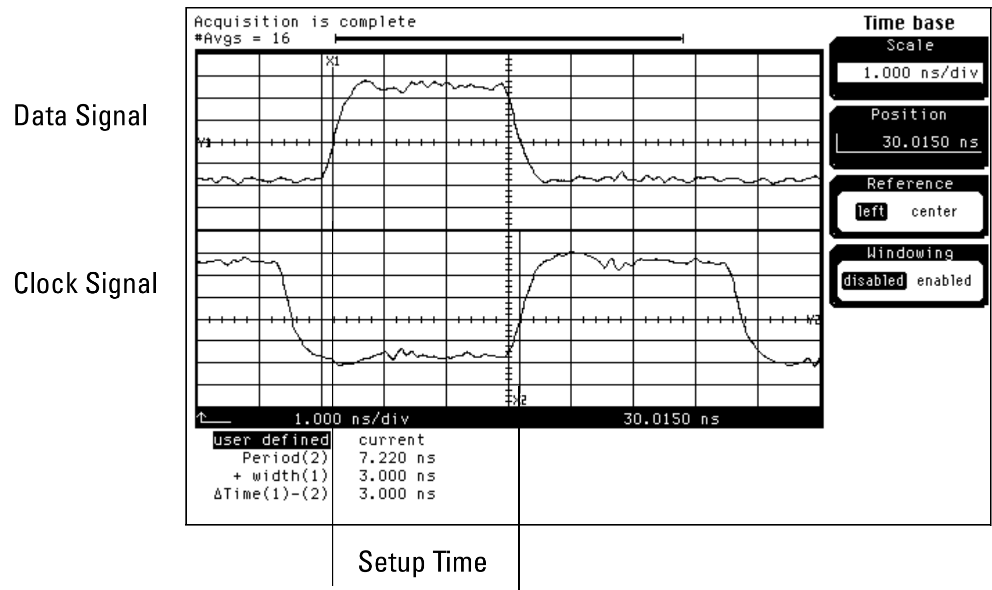
3 **Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.**

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

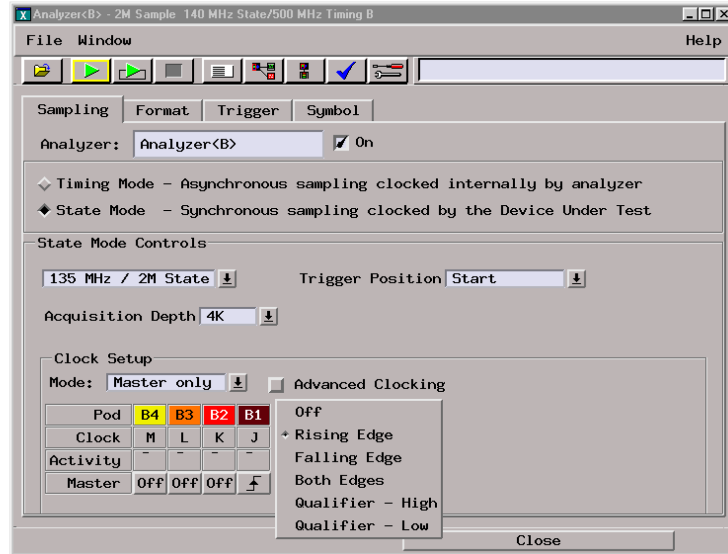


Disregard the Period(2) value. The settings provided in this procedure measure the period from falling edge to falling edge, which is not a valid measurement.

4 Select the clock to be tested.

a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select the clock edge field under the clock to be tested. Then select Rising Edge.



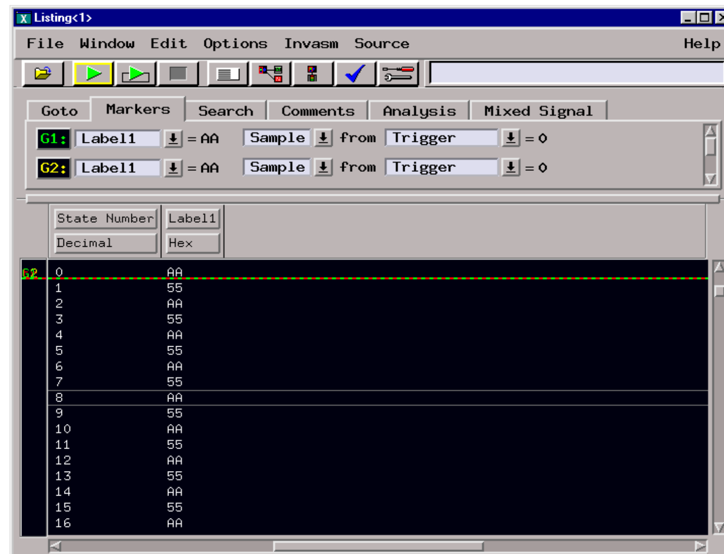
Clocks

J↑	K↑	L↑	M↑

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

5 Verify the test data.

a In the Listing window, select the Run icon. The display should show an alternating pattern of “AA” and “55”.

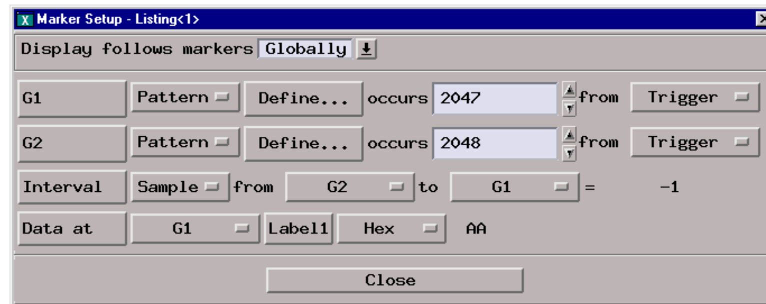


b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter “aa”. Select Apply, then select Close.

c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter “55”. Select Apply, then select Close.

d In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G1. Enter 2047.

e In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the “Pattern NOT found for marker…” error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Repeat steps 4 and 5 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

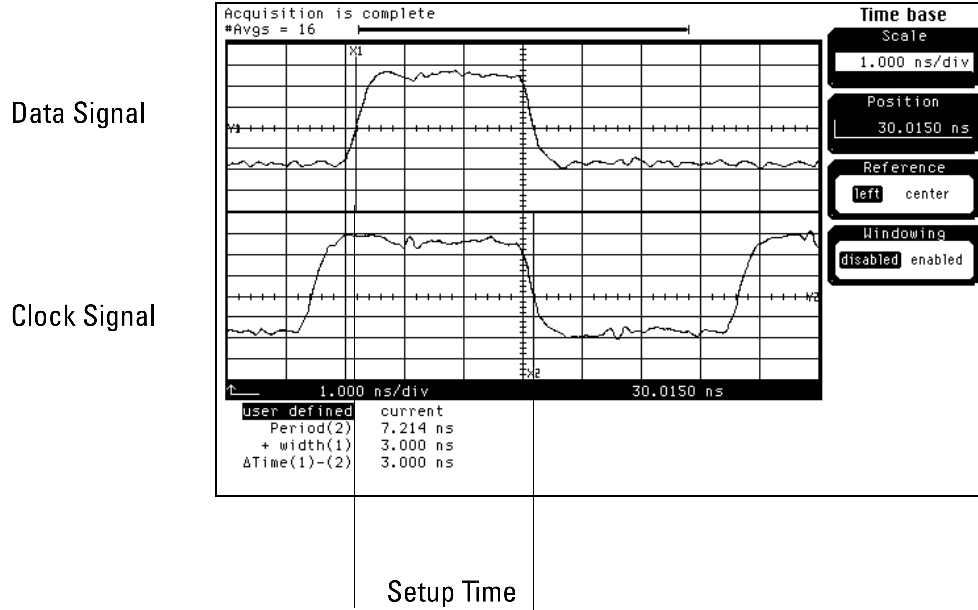
7 Enable the pulse generator channel 1 COMP (LED on).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: falling.

b On the oscilloscope, select [Shift] ΔTime. Select Start src: channel 1, then select [Enter] to display the setup time (ΔTime(1)-(2)).

c Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

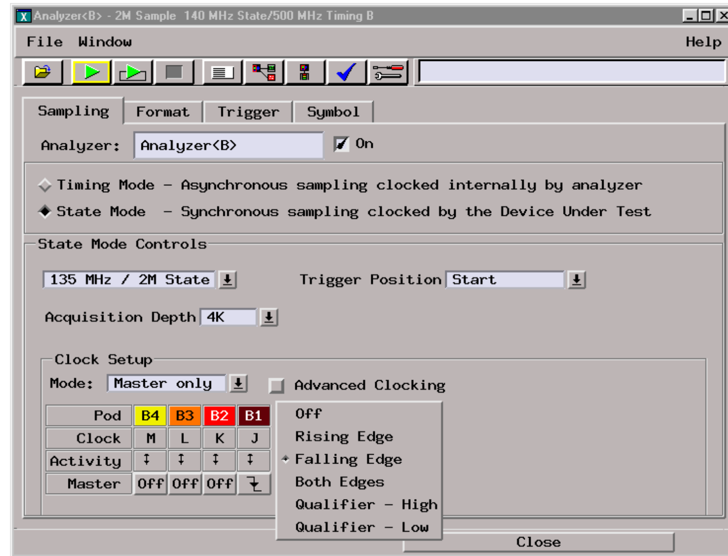


Disregard the Period(2) value. The settings provided in this procedure measure the period from rising edge to rising edge, which is not a valid measurement.

9 Select the clock to be tested.

a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select the clock edge field under the clock to be tested. Then select Falling Edge. The first time through this test, select the first clock and edge. Ensure all other clocks are turned off.



Clocks

J↓	K↓	L↓	M↓

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

10 Verify the test data.

a In the Listing window, select the Run icon. The display should show an alternating pattern of “AA” and “55”.

b If the “Pattern NOT found for marker...” error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

11 If the setup/hold used for the previous steps was 3.0/0.0 ns, repeat steps 1 through 11 using setup/hold -0.5/3.5 ns. If the setup/hold used for the previous steps was -0.5/3.5 ns, continue on with the next section.

To Test the Multiple-clock, Multiple-edge, State Acquisition

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

This test checks a combination of data channels using multiple clocks at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Pulse Generator	140 Mhz, 3.0 ns pulse width, $<$600 ps rise time	8133A option 003
Digitizing Oscilloscope	$\geq$ 6 GHz bandwidth, $<$ 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC (m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

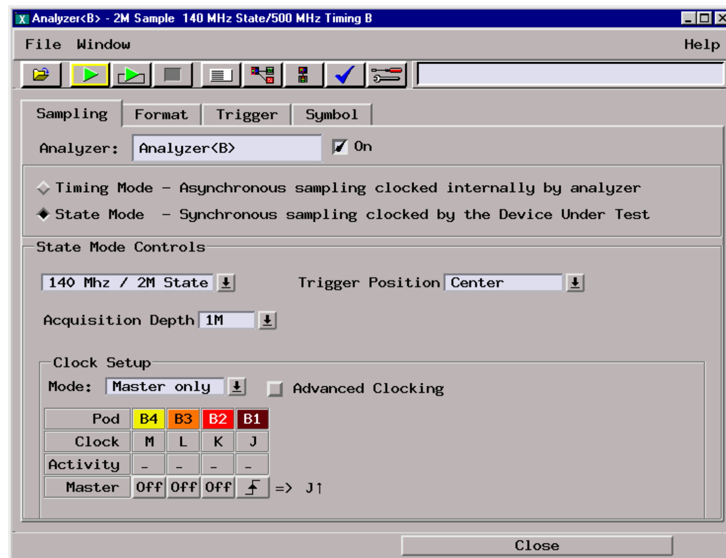
1. If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 35. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.
2. Change the pulse generator channel 2 width to 4.000 ns.

Set up the logic analyzer

Perform the following steps if you have not already done so for the previous test.

1. Set up the Sampling tab.
   a. In the Analyzer window, select the Sampling tab.
   b. Select State Mode.

c Select the 135MHz/2M state mode field, then select 140MHz/2M state.

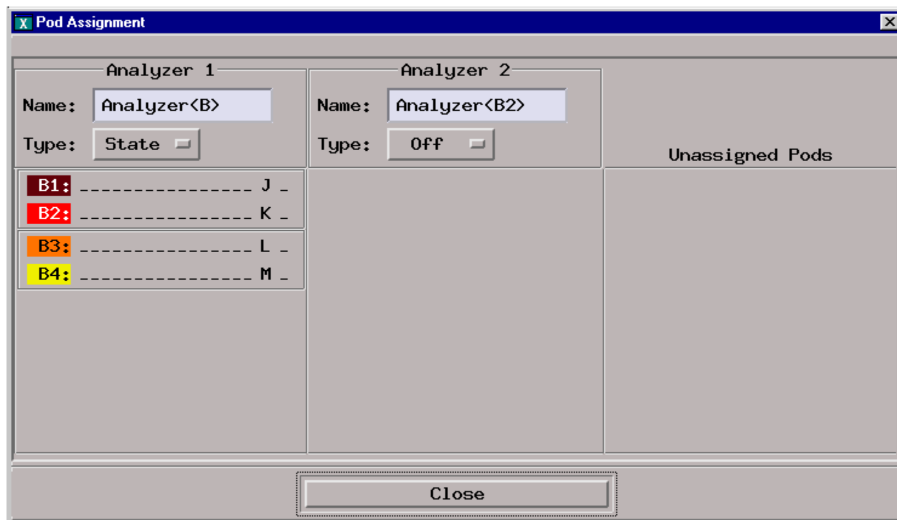


2 Assign all pods to Analyzer 1.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods to the Analyzer 1 column.



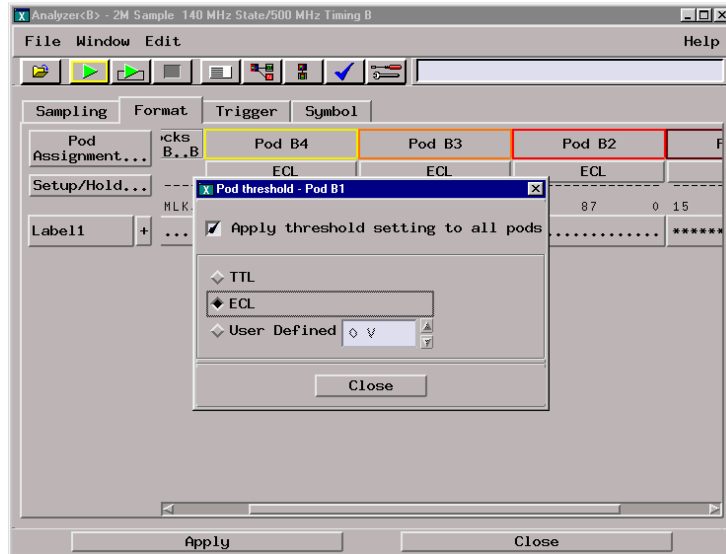
d Select Close to close the Pod Assignment window.

3 Set up the Format tab.

a Under one of the pod fields, select TTL.

b In the Pod Threshold window, ensure the Apply threshold setting to all pods checkbox is checked.

c In the Pod Threshold window, select ECL.



d Select Close to close the Pod Threshold window.

4 Set up the Trigger tab.

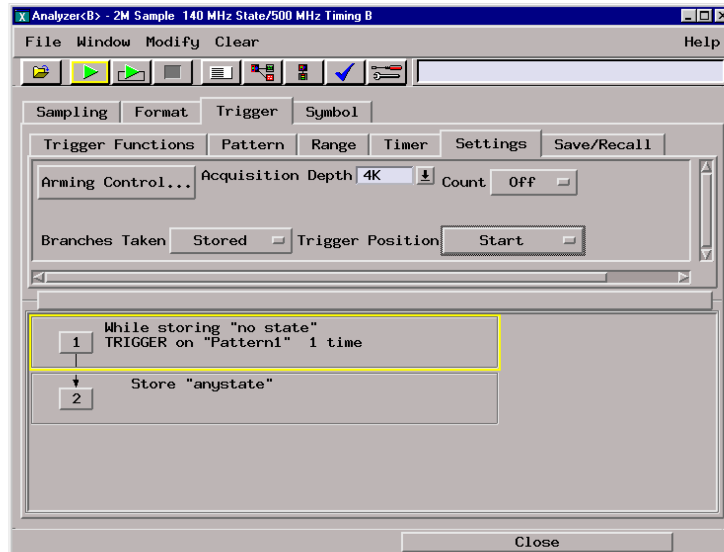
a In the Analyzer setup window, select the Trigger tab. Under the Trigger tab, select the Settings tab.

b Select the Acquisition Depth field, then select “4K”.

c Select the Count field, then select “Off”.

d Select the Trigger Position field, then select Start.

e Select the field labeled “1” in the Sequence field, then at the pop-up menu select Edit. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.

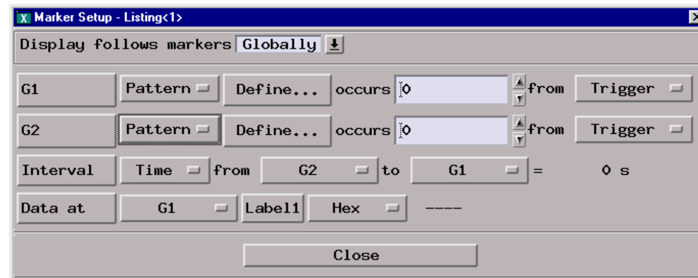


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window appears.

c Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

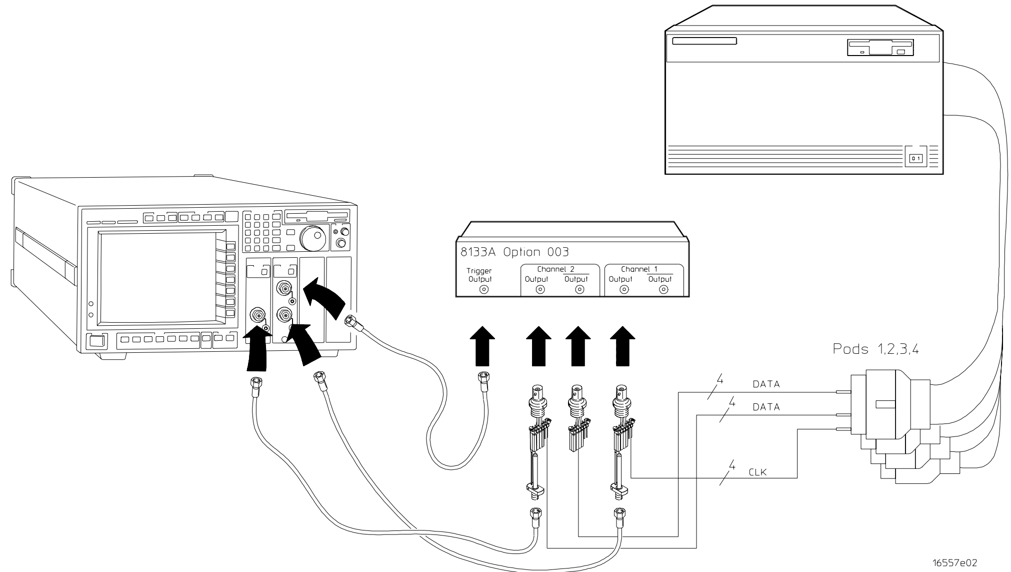


Note: Leave the Marker Setup window open. You will be entering numeric values in the “occurs” field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following table to the pulse generator.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration.



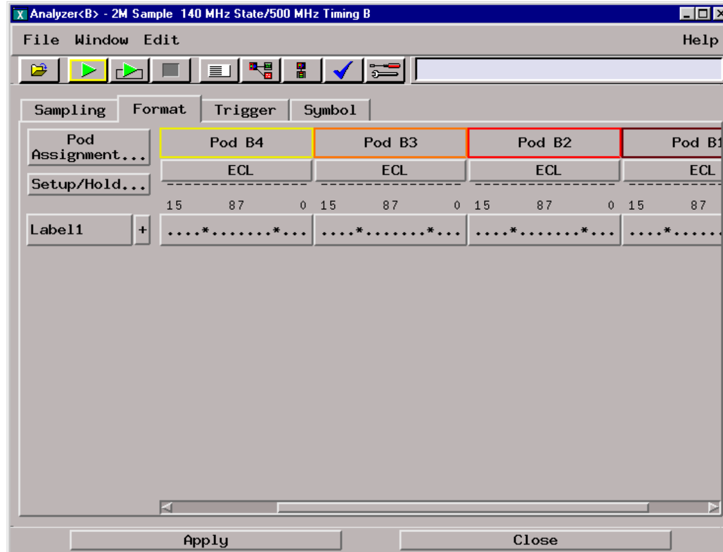
Connect the 16557D to the Pulse Generator

Agilent 8133A Ch2 Output	8133A Ch2 $\overline{\text{Output}}$	8133A Ch1 Output
Pod 1 channel 3	Pod 1 channel 11	J-clock
Pod 2 channel 3	Pod 2 channel 11	K-clock
Pod 3 channel 3	Pod 3 channel 11	L-clock
Pod 4 channel 3	Pod 4 channel 11	M-clock

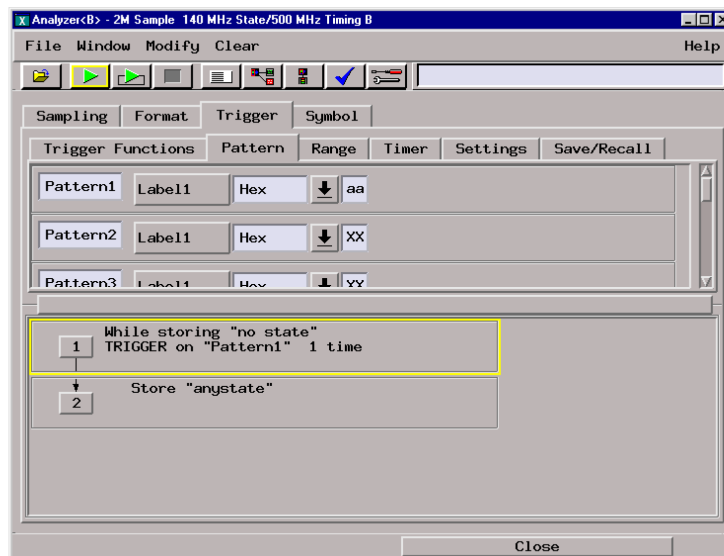
3 Activate the data channels that are connected according to the previous table.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select the data channels to be tested (channels 11 and 3 of each pod). An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



c Under the Trigger tab, select the Pattern tab. Under the Pattern tab, select the pattern field associated with pattern recognizer “Pattern 1”. Enter “aa”.



Verify the test signal

1 **Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 7.142 ns, +0 ps or -142 ps.**

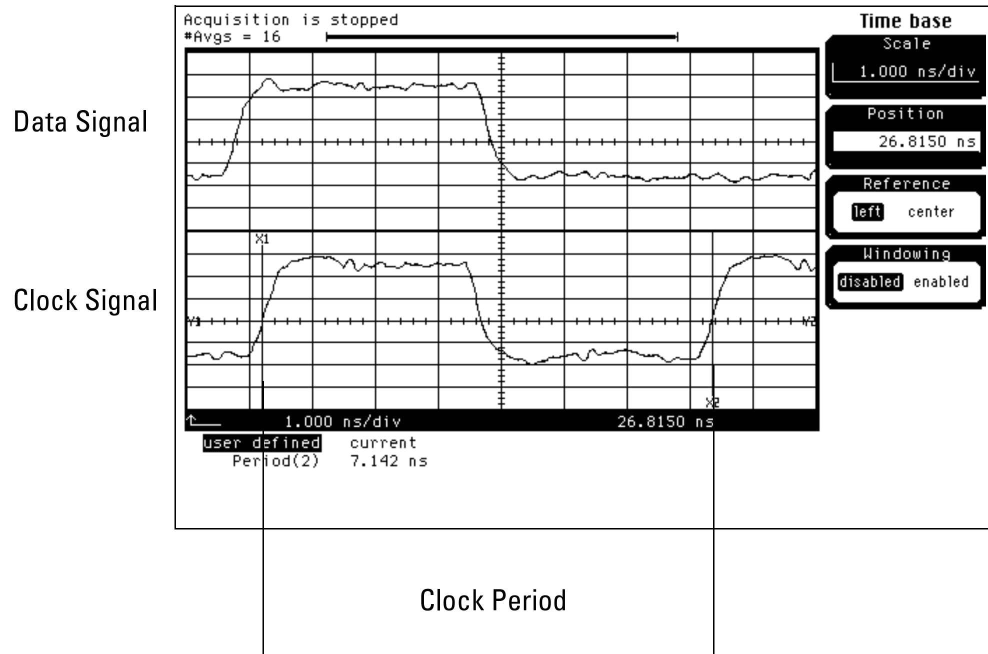
a Turn on the pulse generator channel 1, channel 2, and trigger outputs.

b In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

d On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 7.142 ns, go to step e. If the period is less than or equal to 7.142 ns but greater than 7.000 ns, go to step 2.

e In the oscilloscope Timebase menu, increase Position 7.142 ns. If the period is more than 7.142 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than or equal to 7.142 ns but greater than 7.000 ns.



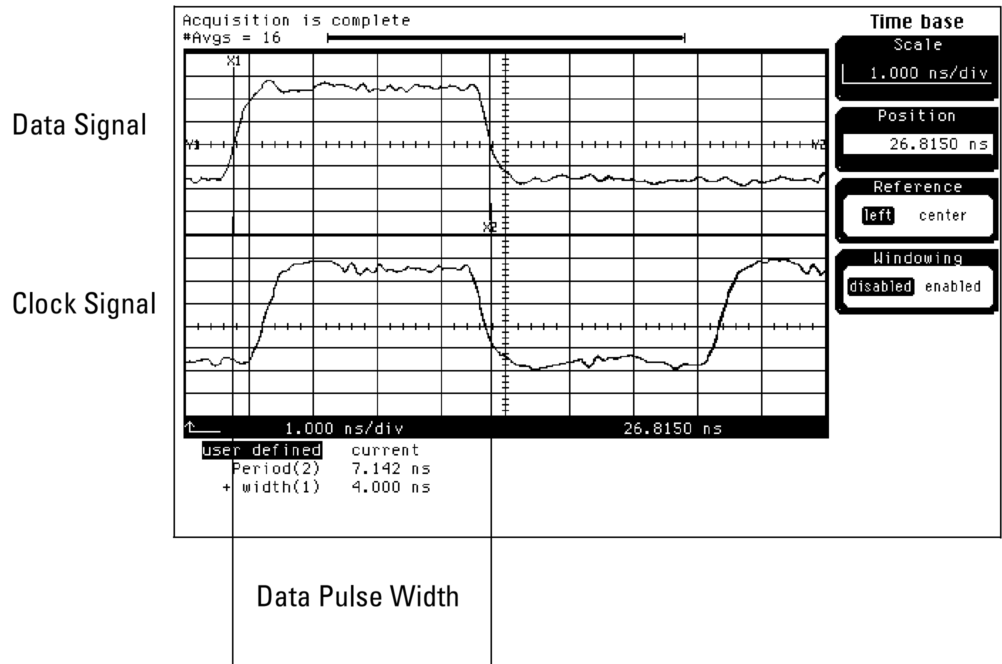
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or - 100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width (1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock edges, multiple clocks

1 Select the logic analyzer setup/hold time.

a In the Analyzer setup window, select the Sampling tab.

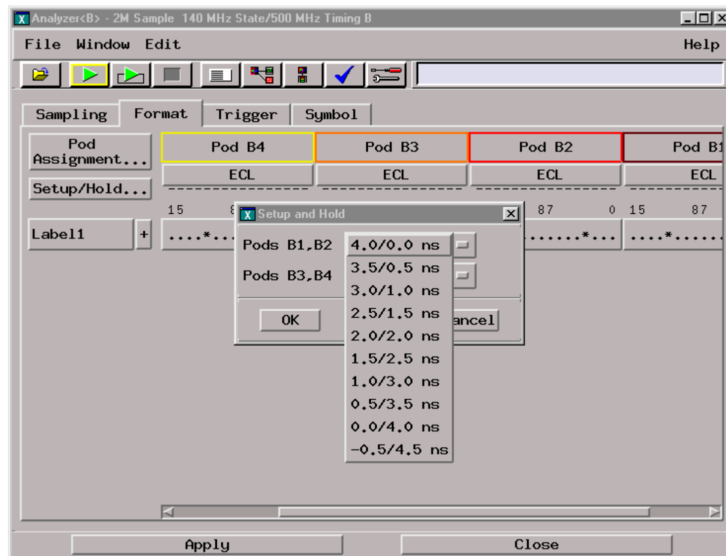
b Under the Sampling tab, select and activate any two clock edges, then select OK.

You must have two single-edge clocks selected before the Setup/Hold window will allow a Setup/Hold of 4.0/0.0 ns.

c Set the Format tab. Under the Format tab, select Setup/Hold.

d In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations
4.0/0.0 ns
-0.5/4.5 ns



e Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

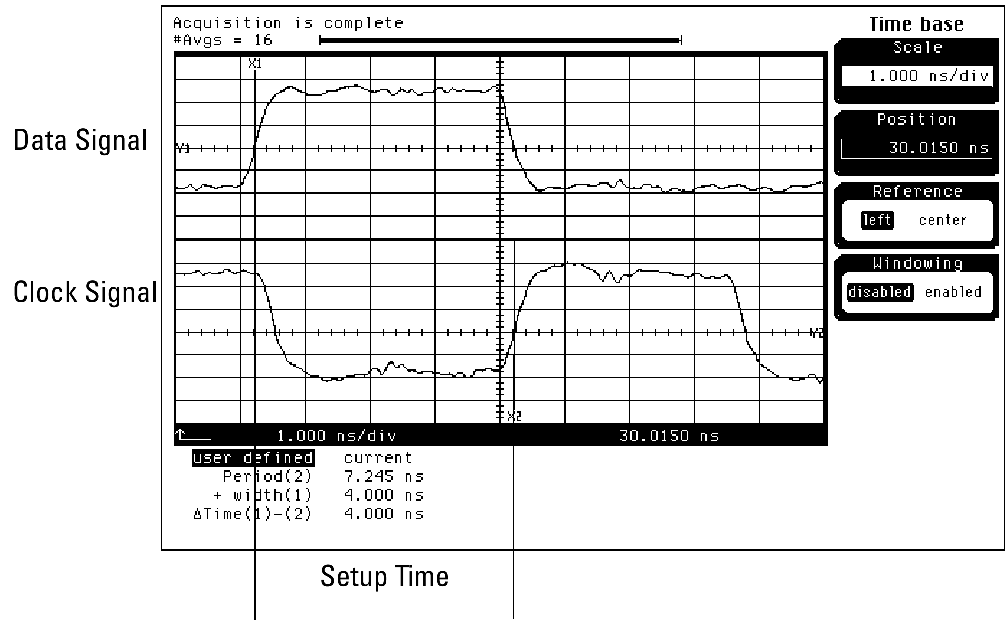
3 **Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.**

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

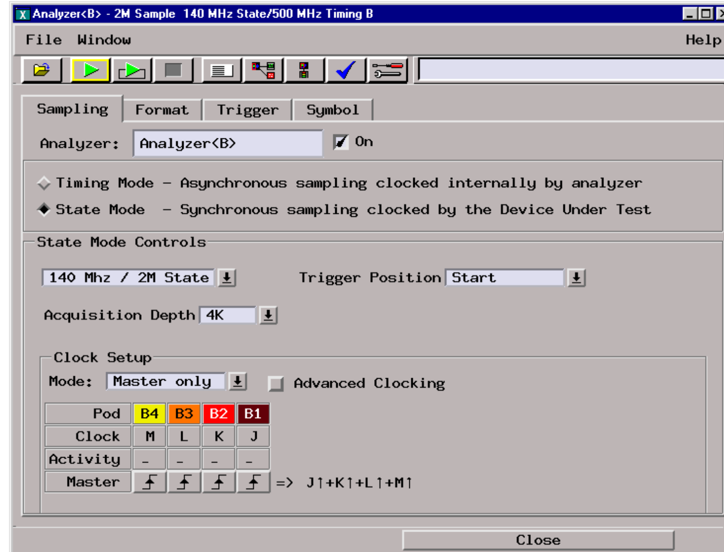


Disregard the Period(2) value. The settings provided in this procedure measure the period from falling edge to falling edge, which is not a valid measurement.

4 Select the clock combination to be tested.

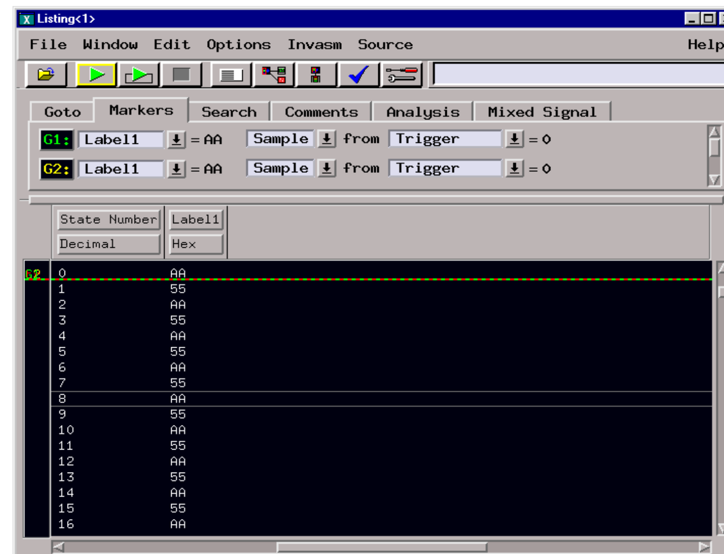
a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select the clock edge field under each clock. Then select Rising Edge. The clock setup field should show: J↑ + K↑ + L↑ + M↑.

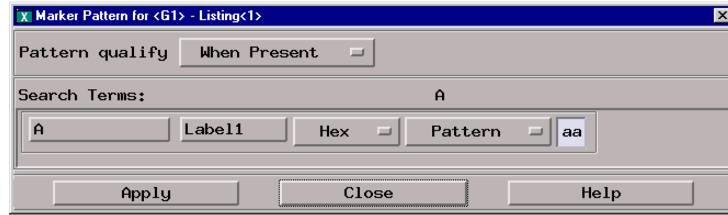


5 Verify the test data.

a In the Listing window, select the Run icon. The display should show an alternating pattern of "AA" and "55".



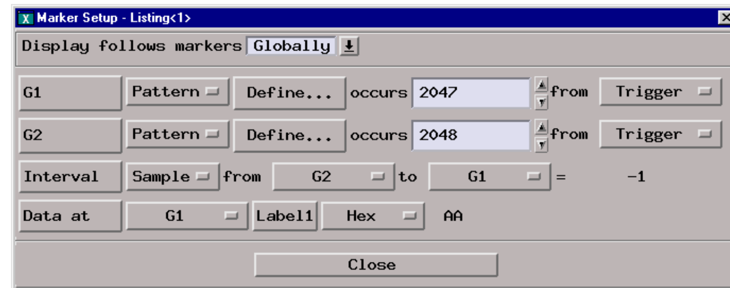
b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter “aa”. Select Apply, then select Close.



c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter “55”. Select Apply, then select Close.

d In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G1. Enter 2047.

e In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the “Pattern NOT found for marker...” error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Repeat steps 4, 5, and 6 for the next clock edge combination listed in the table in step 4, until both clock combinations have been tested.

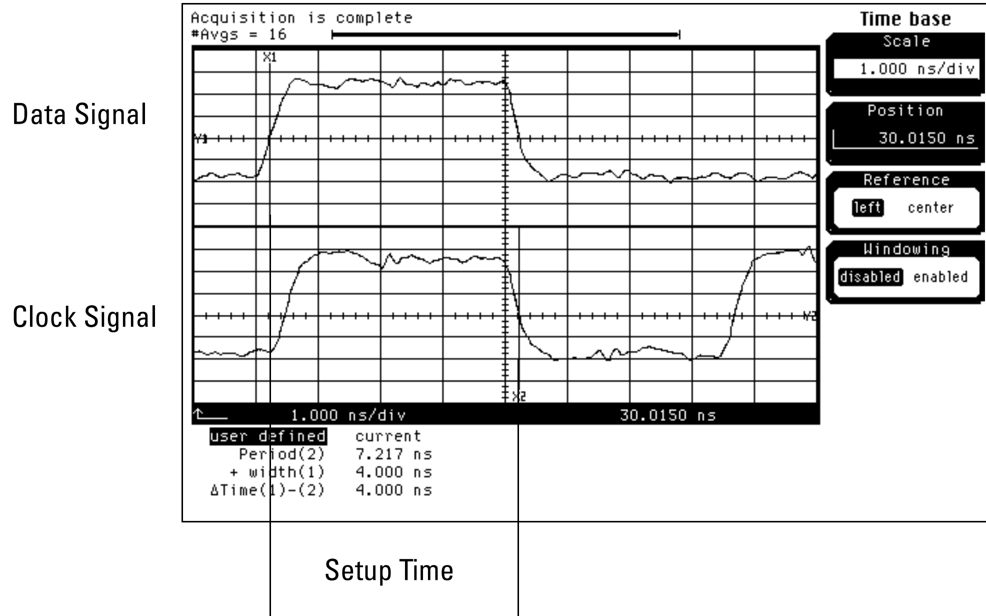
7 Enable the pulse generator channel 1 COMP (LED on).

8 **Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.**

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: falling.

b On the oscilloscope, select [Shift] ΔTime. Select Start src: channel 1, then select [Enter] to display the setup time (ΔTime(1)-(2)).

c Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

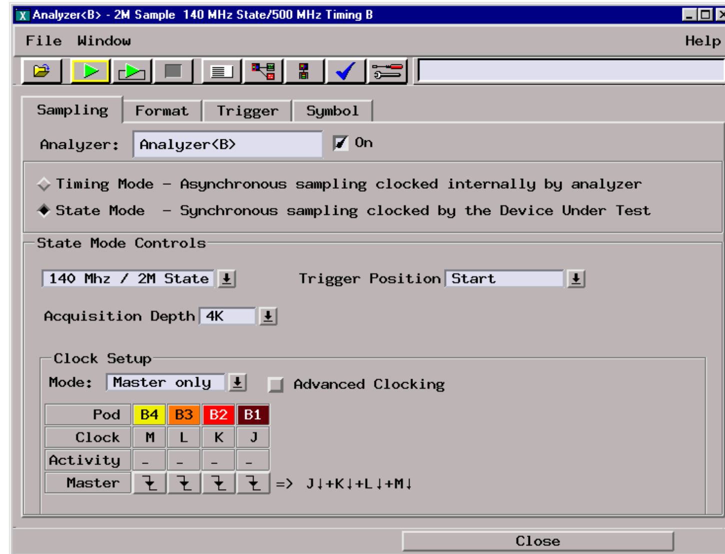


Disregard the Period(2) value. The settings provided in this procedure measure the period from rising edge to rising edge, which is not a valid measurement.

9 Select the clock combination to be tested.

a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select the clock edge field under each clock. Then select Falling Edge. The clock setup should show: J↓ + K↓ + L↓ + M↓.



10 Verify the test data.

a In the Listing window, select the Run icon. The display should show an alternating pattern of "AA" and "55".

b If the "Pattern NOT found for marker..." error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

11 Repeat steps 9, 10, and 11 for the next clock combination listed in the table in step 9, until both clock combinations have been tested.

12 If the setup/hold used for the previous steps was 4.0/0.0 ns, repeat steps 1 through 11 using setup/hold -0.5/4.5 ns. If the setup/hold used for the previous steps was -0.5/4.5 ns, continue on with the next section.

To Test the Single-clock, Multiple-edge, State Acquisition

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

This test checks a combination of data channels using a multiple-edge single clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/ Part
Pulse Generator	140 Mhz, 3.0 ns pulse width, <600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC (m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

1 If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 35. Use the pulse generator settings listed below.

2 Make the following changes to the pulse generator configuration.

Timebase	Channel2
Period: 14.284 ns	Divide: PULSE ÷ 1 Width: 3.500 ns

Set up the logic analyzer

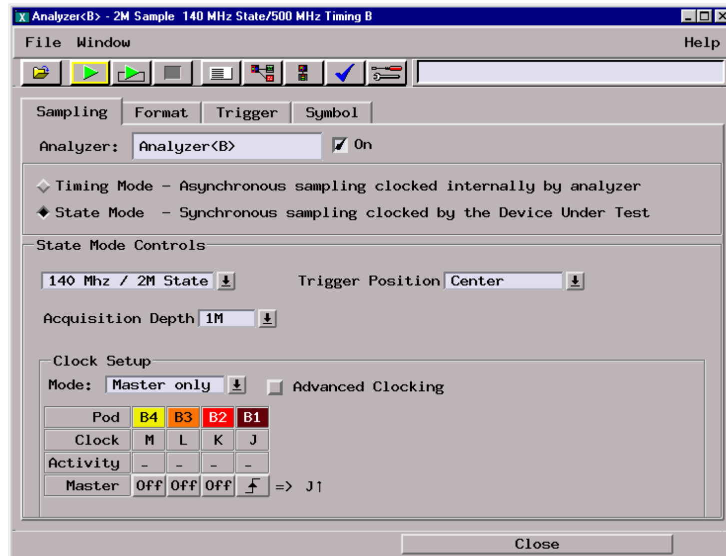
Perform the following steps if you have not done so for the previous tests.

1 Set up the Sampling tab.

a In the Analyzer window, select the Sampling tab.

b Select State Mode.

c Select the 135MHz/2M state mode field, then select 140MHz/2M state.

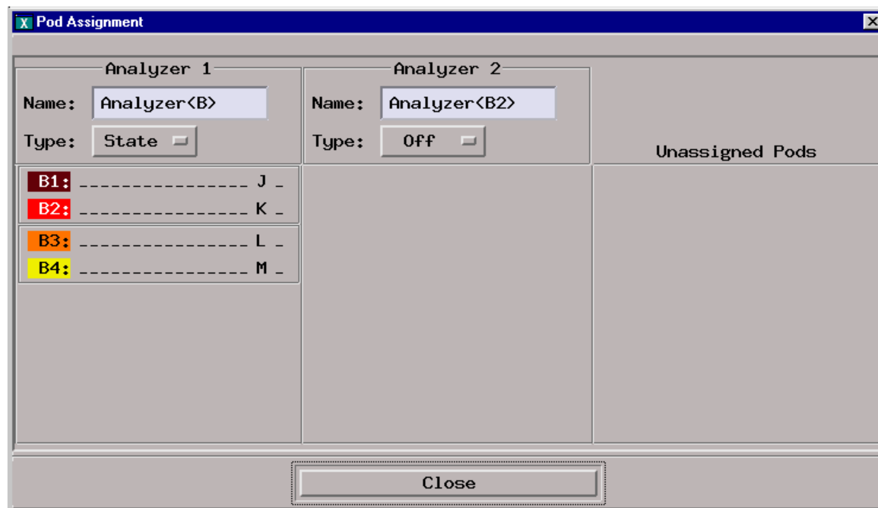


2 Assign all pods to Analyzer 1.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods to the Analyzer 1 column.



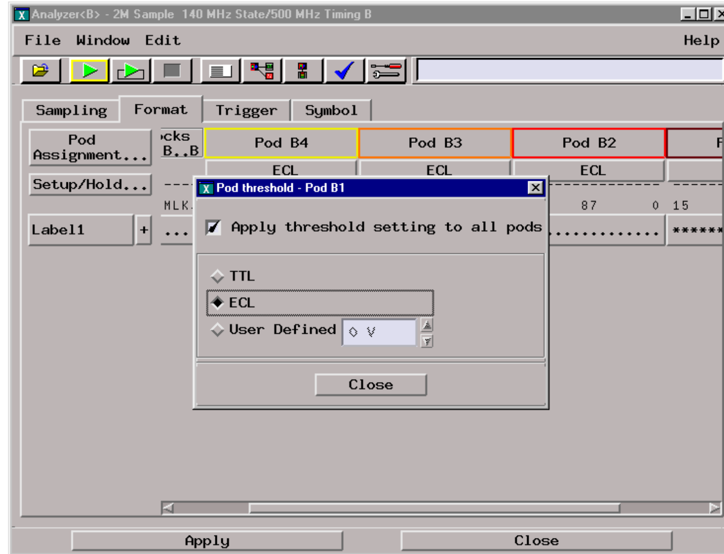
d Select close to close the Pod Assignment window.

3 Set up the Format tab.

a Under one of the pod field, select TTL.

b In the Pod Threshold window, ensure the Apply threshold setting to all pod checkbox is checked.

c In the Pod Threshold window, select ECL.



d Select Close to close the Pod Threshold window.

4 Set up the Trigger tab.

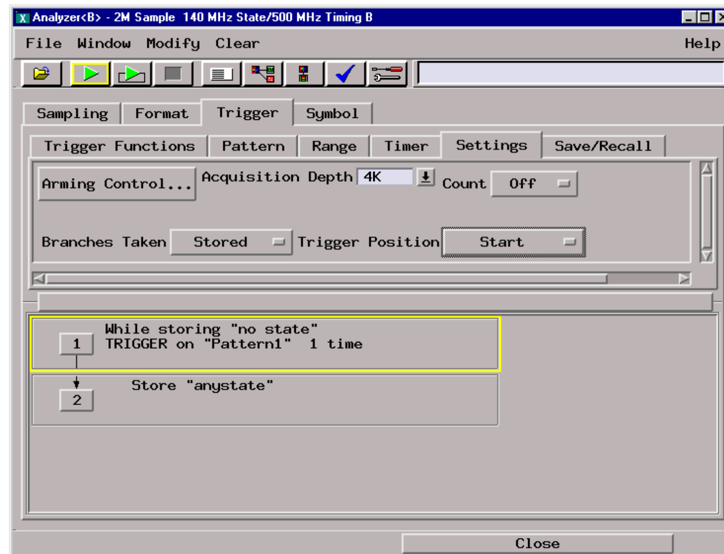
a In the Analyzer setup window, select the Trigger tab. Under the Trigger tab, select the Settings tab.

b Select the Acquisition Depth field, then select “4K”.

c Select the Count field, then select “Off”.

d Select the Trigger Position field, then select Start.

e Select the field labeled “1” in the Sequence field, then at the pop-up menu, select Edit. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.

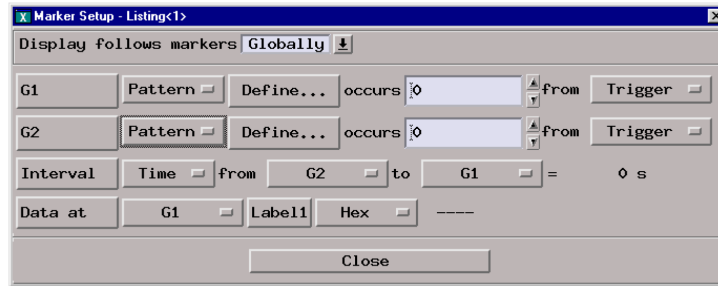


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window appears.

c Select the Sample field associated with G1, and select Pattern. Select the Sample field associated with G2, and select Pattern.

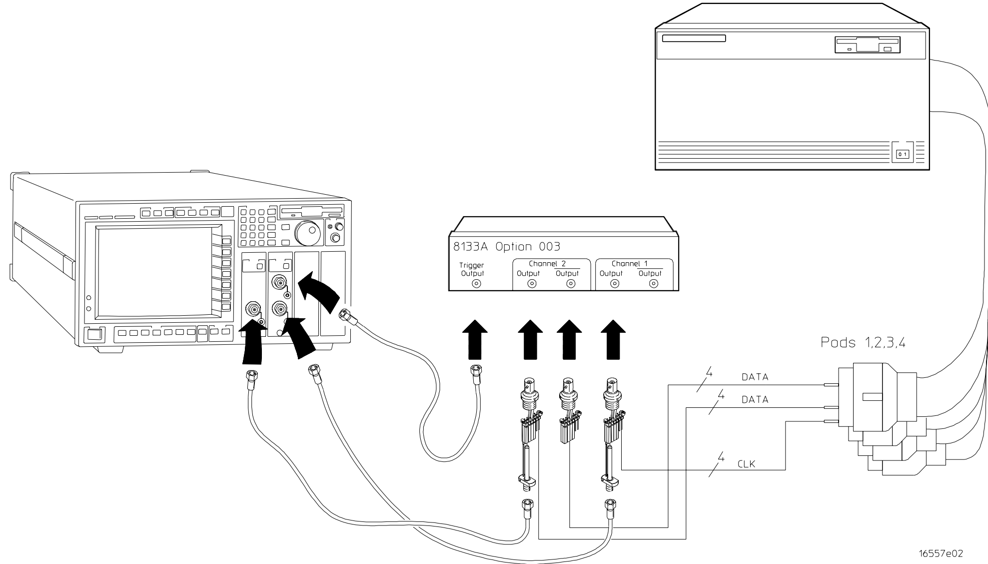


Note: Leave the Marker Setup window open. You will be entering numeric values in the “occurs” field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration.



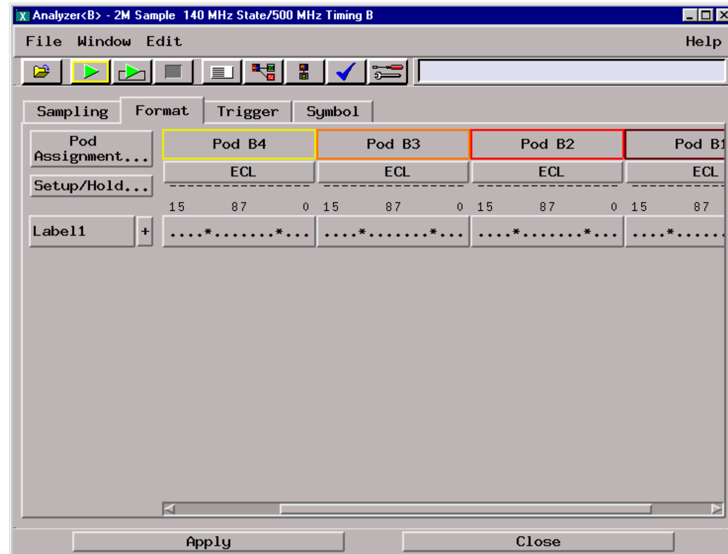
Connect the 16557D to the Pulse Generator

Agilent 8133A Ch2 Output	8133A Ch2 $\overline{\text{Output}}$	8133A Ch1 Output
Pod 1 channel 3	Pod 1 channel 11	J-clock
Pod 2 channel 3	Pod 2 channel 11	
Pod 3 channel 3	Pod 3 channel 11	
Pod 4 channel 3	Pod 4 channel 11	

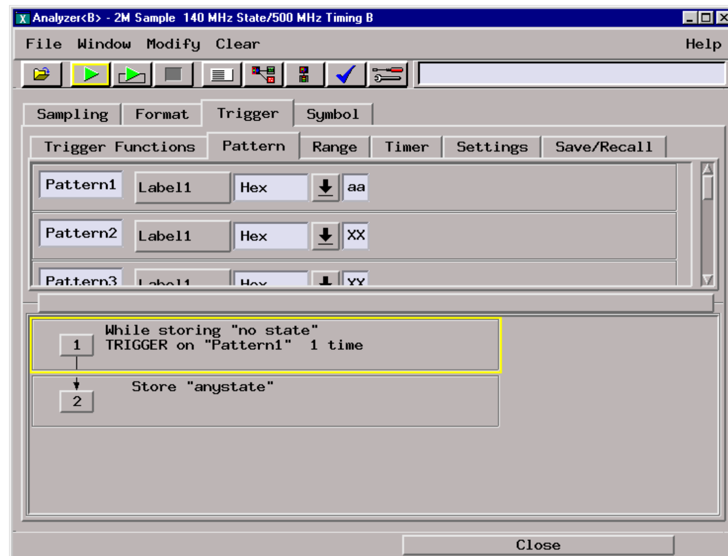
3 Activate the data channels that are connected according to the previous table.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for one of the pods being tested, then select Individual. Using the mouse, select the data channels to be tested (channels 11 and 3 of each pod). An asterisk means that a channel is turned on. Follow this step for the remaining pods to be tested.



c Under the Trigger tab, select the Pattern tab. Under the Pattern tab, select the pattern field associated with pattern recognizer "Pattern1". Enter "aa".



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 7.142 ns, +0 ps or -142 ps.

a Turn on the pulse generator channel 1, channel 2, and trigger outputs.

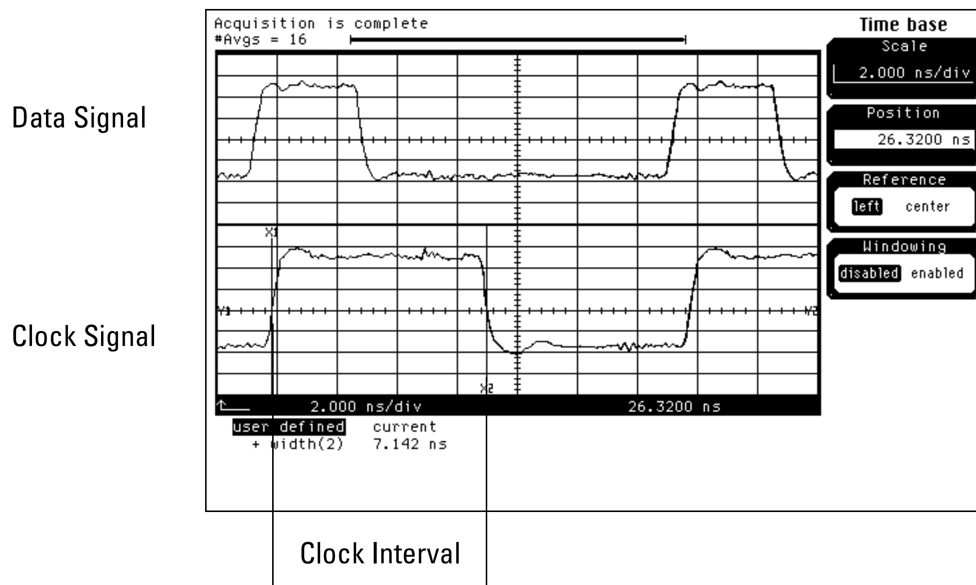
b In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

d On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 7.142 ns, go to step e. If the positive-going pulse width is less than or equal to 7.142 ns but greater than 7.000 ns, go to step 2.

e On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 7.142 ns but greater than 7.000 ns, go to step 2.

f Decrease the pulse generator Period in 10-ps increments until the oscilloscope + width (2) or - width (2) read less than or equal to 7.142 ns, but greater than 7.000 ns.



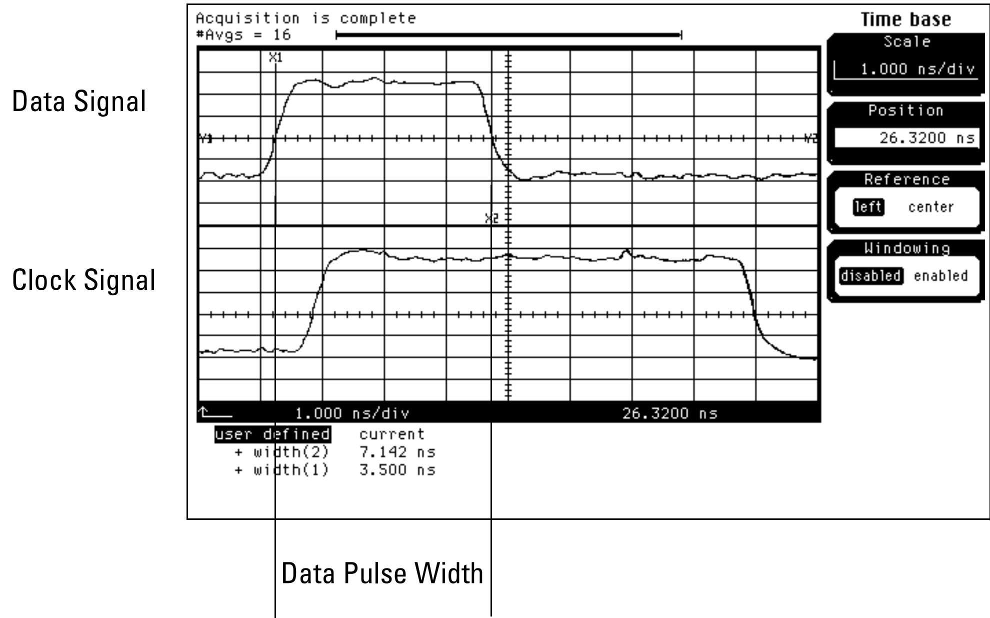
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.500 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock, multiple clock edges

1 Select the logic analyzer setup/hold time.

a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select and activate a rising and falling edge for any clock.

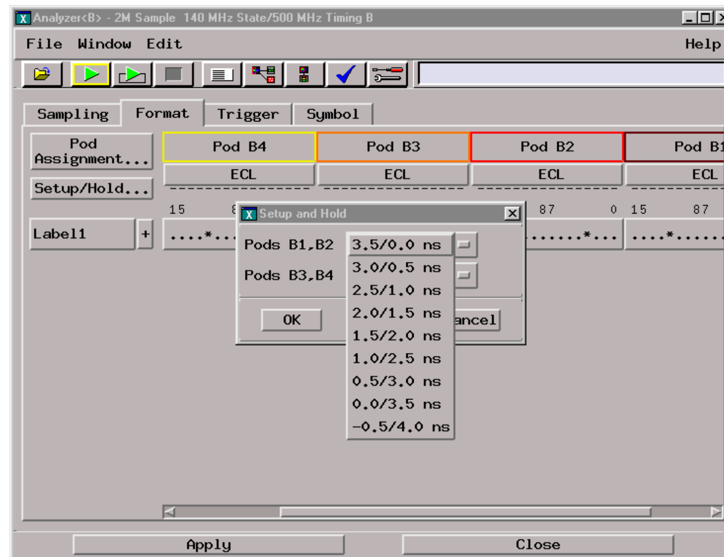
The Setup/Hold window requires a double clock edge before it will allow a setup/hold of 3.5/0.0 ns.

c Under the Format tab, select Setup/Hold.

d In the Setup/Hold window, select the setup/hold field next to each pod pair, then select the setup/hold combination to be tested. Repeat for all pods. The first time through this test, select the top combination in the following table.

Setup/Hold Combinations

3.5/0.0 ns
-0.5/4.0 ns



e Select OK to exit the Setup/Hold window.

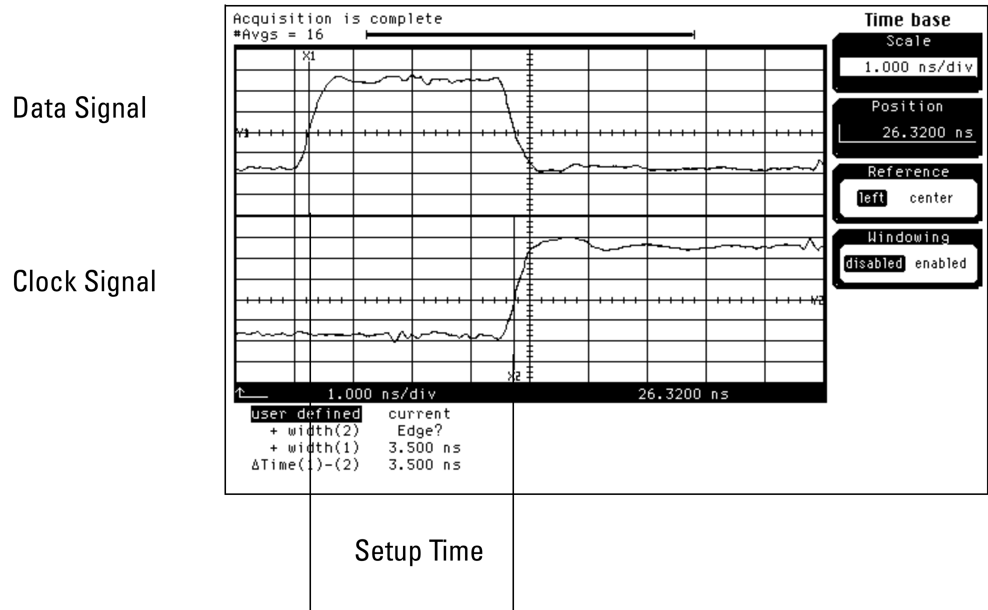
2 **Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.**

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

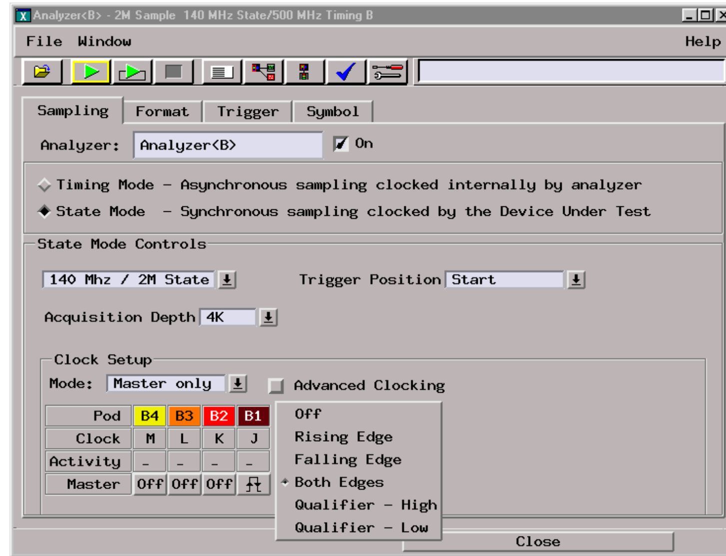
d Adjust the pulse generator channel 2 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



3 Select the clock to be tested.

a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select the clock edge field under the clock to be tested. Then select Both Edges. Ensure all other clock are turned off.



Clocks

J↕	K↕	L↕	M↕

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

4 Verify the test data.

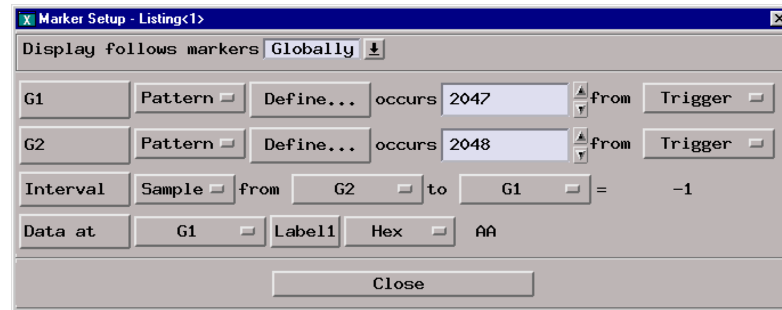
a In the Listing window, select the Run icon. The display should show an alternating pattern of “AA” and “55”.

b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter “aa”. Select Apply, then select Close.

c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter “55”. Select Apply, then select Close.

d In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G1. Enter 2047.

e In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the “Pattern NOT found for marker...” error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

5 Repeat steps 3, 4, and 5 for the next clock edge listed in the table in step 3, until all listed clock edges have been tested.

6 If the setup/hold used for the previous steps was 3.5/0.0 ns, repeat steps 1 through 5 using setup/hold -0.5/4.0 ns. If the setup/hold used for the previous steps was -0.5/4.0 ns, continue on with the next section.

To Test the Time Interval Accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

This test verifies that the 125-MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 Mhz, 3.5 ns pulse width, $<$600 ps rise time	8133A Option 003
Function Generator	Accuracy $\leq (5)(10^{-6})$ x frequency	8656B Option 002
SMA Coax Cable	18 GHz Bandwidth	8120-4948
BNC Cable		8120-1840
Adapter	SMA(m)-BNC(f)	1250-1200
Adapter	BNC(m)-SMA(f)	1250-2015
Coupler	BNC(m-m)	1250-0216
BNC Test Connector, 6x2		

Set up the equipment

1 If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 35.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger
Mode: Ext Period: 25.000 ns	Mode: Square Delay: 0.000 ns High: -0.90 V Low: -1.70 V COMP: Disabled (LED Off)	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V

3 Set up the function generator according to the following table.

Function Generator Setup

Freq: 40.000 00 MHz	Amptd: 1.00 V	Modulation: Off

Set up the logic analyzer

1 Set up the Sampling tab.

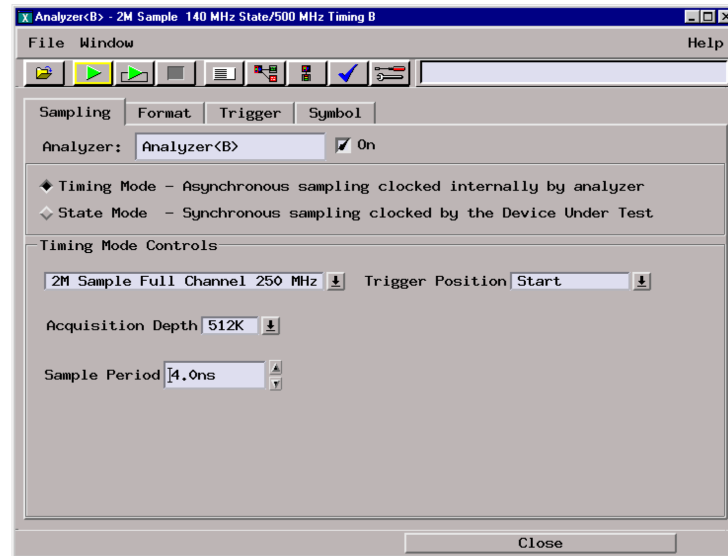
a In the Analyzer setup window, select the Sampling tab.

b Select Timing Mode.

c In the Timing Mode Controls, select Trigger Position. Then select Start.

d Select the Acquisition Depth field. Then select “512K”.

e Select the sample period field. Then enter 4.0 ns.



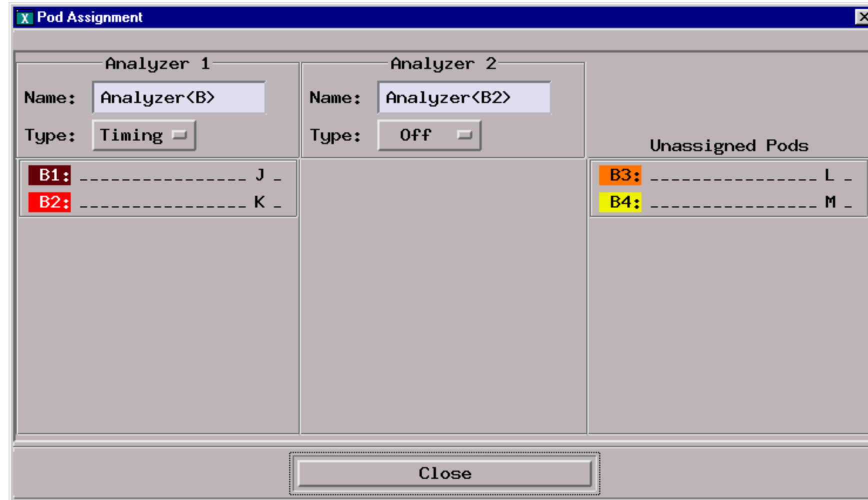
2 Set up the Format tab.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag Pods 1 and 2 to the Analyzer 1 column. Use the mouse to drag Pods 3 and 4 to the Unassigned column.

d Select Close to close the Pod Assignment window.



e Under the Format tab, select the field showing the channel assignments for Pod 1. Using the mouse, first clear the channels (all "."), then select channel 0. An asterisk means that the channel is turned on.

f Under the Pod 1 field, select TTL, then select ECL.

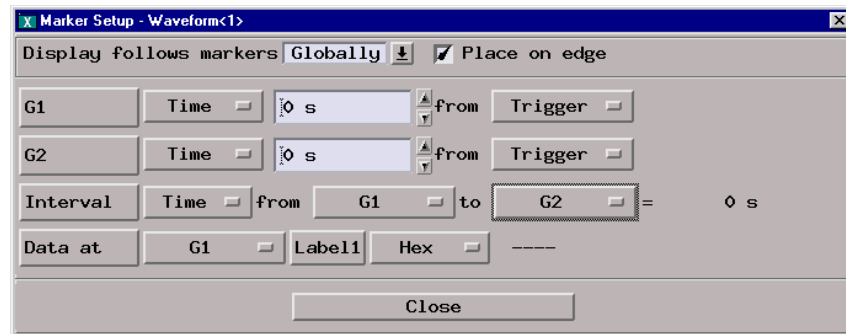
3 Set up the Waveform window.

a In the Analyzer setup window, select Window, then select Slot n: Analyzer<n> (where "n" is the slot you have the module installed), then select Waveform. A Waveform window opens.

b In the Waveform window, select the Markers tab.

c Select the G1 field and a Marker Setup window appears.

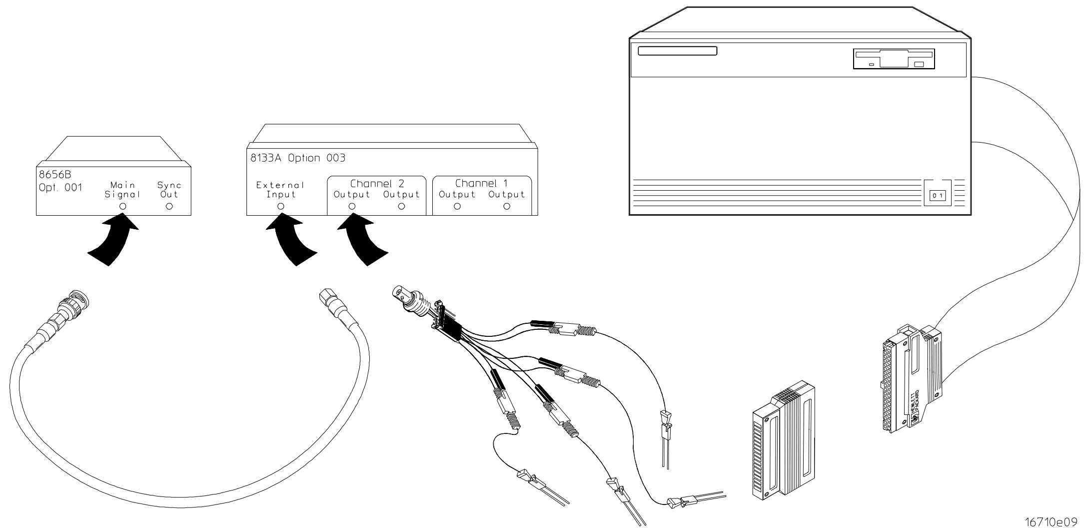
d Ensure that the Interval Time field reads “from G1 to G2” (instead of “from G2 to G1”).



Leave this window open as you will be using it later when acquiring data.

Connect the logic analyzer

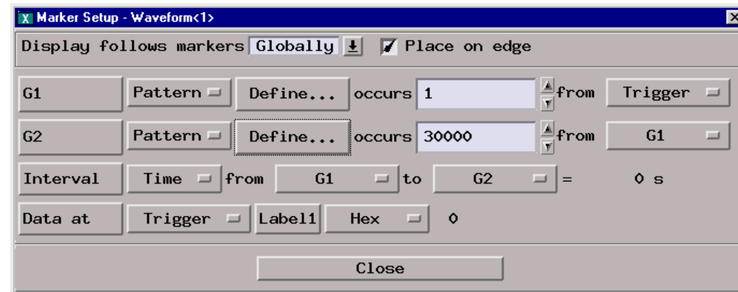
1. Using a 6-by-2 test connector, connect channel 0 of Pod 1 to the pulse generator channel 2 output.
2. Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



Acquire the data

1. Enable the pulse generator channel 2 and trigger outputs (with the LED off).
2. In the logic analyzer Waveform window, select the Run icon.
3. Configure the Markers to measure the time interval.
   a. In the Marker Setup window select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.
   b. Select the Occurs field associated with G1 and enter “1”. Select the Occurs field associated with G2 and enter “30000”.

c Select the From field associated with G2 and select G1.



In the Marker Setup Window, you will observe the Interval Time from G1 to G2=value to determine the pass or fail status of this test.

d In the marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the Pattern field, enter “1”. Select the Pattern Qualify field and select When Entering. Select Apply, then select Close.

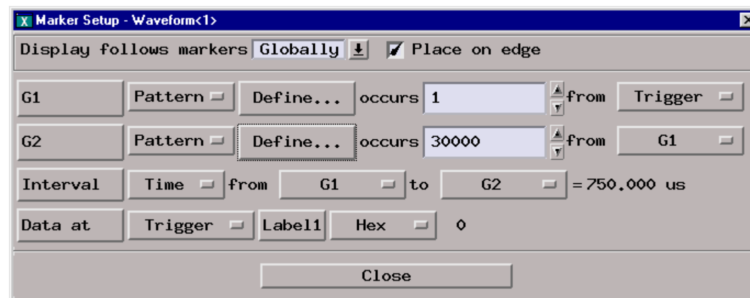
e In the marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the Pattern field, enter “1”. Select the Pattern Qualify field and select When Entering. Select Apply, then select Close.

4 Acquire the data.

a In the Waveform window, move the mouse cursor over Run and click and hold the right mouse button. At the pop-up menu, select Repetitive.

b Select the Run icon. The logic analyzer repetitively acquires data.

c Continuously observe the Interval Time from G1 to G2=value in the Marker Setup window.



Allow the logic analyzer to run repetitively for approximately one minute. If the Interval Time value remains inside the range 749.921 µs to 750.079 µs, the test passes. Record a Pass or Fail in the performance test record.

d Select the Stop icon to end the acquisition.

To Test the Two-, Three-, or Four-card Module

This test is only required for configured two-, three-, or four-card modules. Performing the test verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

Multi-card modules that were changed to one-card modules for the previous performance tests need to be reconfigured as a two-, three-, or four-card module for this test.

This test checks a combination of data channels using a single-edge clock at one selected setup/hold time.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	140 Mhz, 3.0 ns pulse width, $<$600 ps rise time	8133A option 003
Digitizing Oscilloscope	$\geq$ 6 GHz bandwidth, $<$ 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC (m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

Set up the equipment

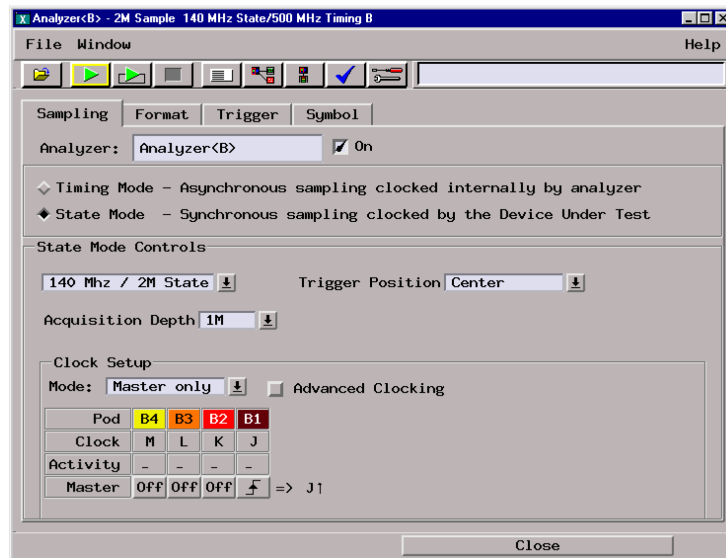
If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 35. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.

Set up the logic analyzer

1 Set up the Sampling tab.

a In the Analyzer window, select the Sampling tab.
b Select State Mode.

c Select the 135 MHz/2M state mode field, then select 140MHz/2M state.

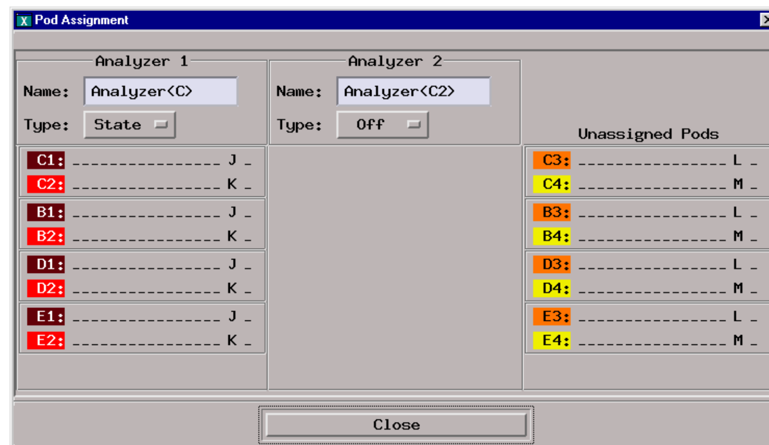


2 Assign pods 1 and 2 of the master card and all expander cards to Analyzer 1.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag pods 1 and 2 to the Analyzer 1 column. Use the mouse to drag pods 3 and 4 to the Unassigned Pods column.



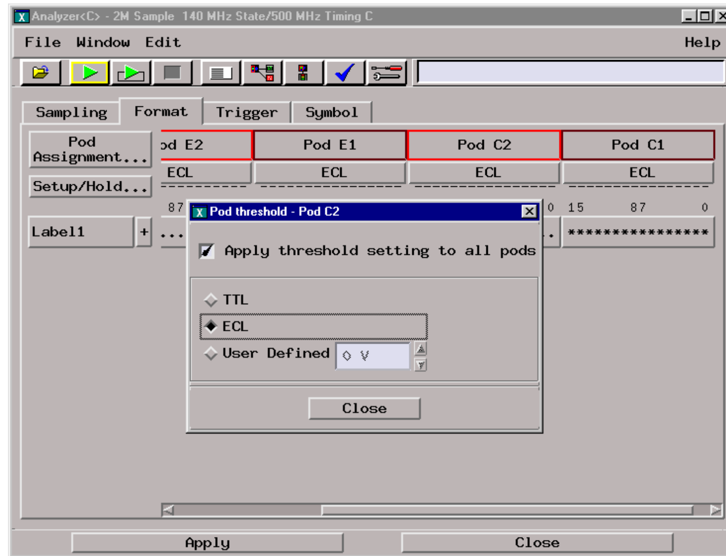
d Select Close to close the pod assignment window.

3 Set up the Format tab.

a Under one of the pod fields, select TTL.

b In the Pod Threshold window, ensure the Apply threshold settings to all pods checkbox is checked.

c In the Pod Threshold window, select ECL.



d Select Close to close the Pod Threshold window.

4 Set up the Trigger tab.

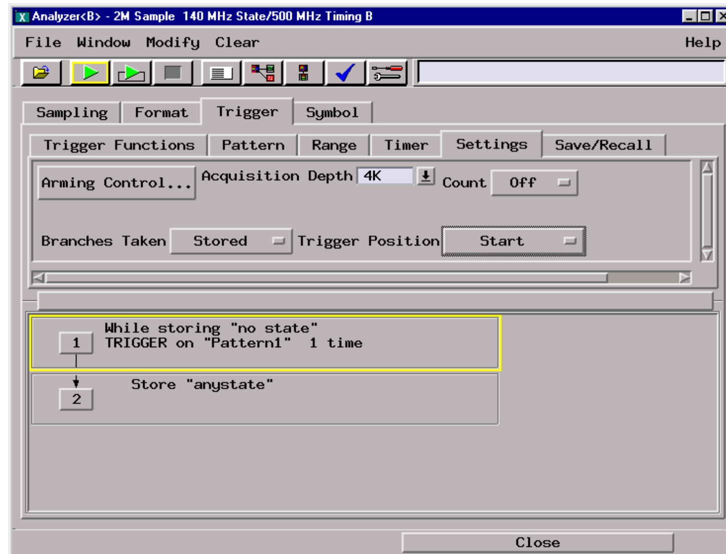
a In the Analyzer setup window, select the Trigger tab. Under the Trigger tab, select the Settings tab.

b Select the Acquisition Depth field, then select “4K”.

c Select the Count field, then select “Off”.

d Select the Trigger Position field, then select Start.

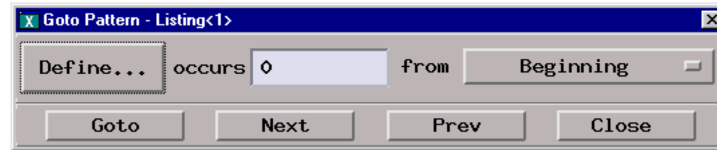
e Select the field labeled “1” in the Sequence field, then at the pop-up menu, select Edit. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.



5 Set up the Listing window.

a In the Listing window, select the Search tab.

b Select the Advanced Searching button, and the Goto Pattern window appears.



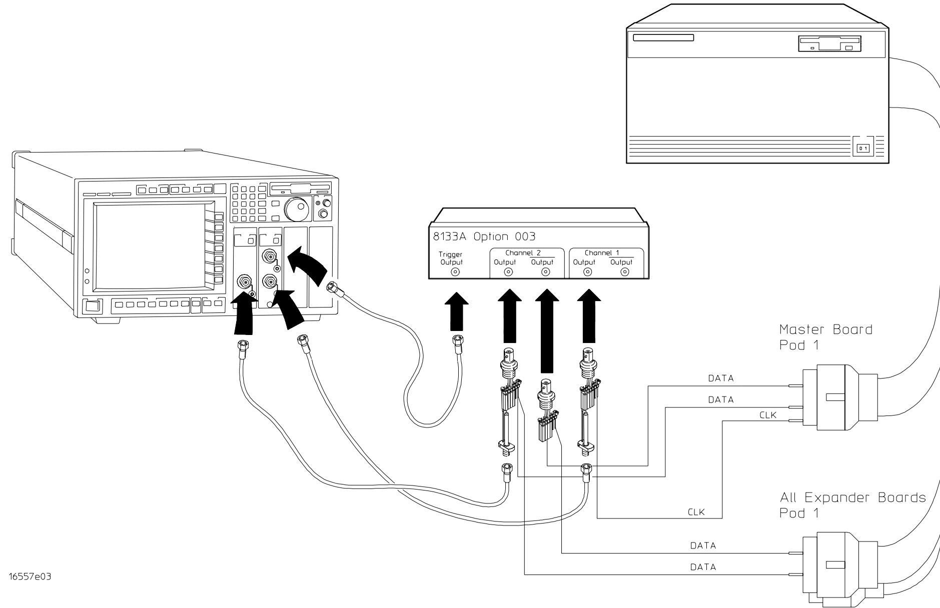
c In the Goto Pattern window, select Define... and the Search Pattern window appears.

Note: Leave these windows open. After you acquire the data you will be entering numeric values in the “occurs” field of the Goto Pattern window and reconfiguring the Search terms in the Search Pattern window.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration.



Connect the 16557D to the Pulse Generator

Agilent 8133A Ch2 Output	8133A Ch2 $\overline{\text{Output}}$	8133A Ch1 Output
Master card		
Pod 1 channel 3	Pod 1 channel 11	J-clock
All Expander cards		
Pod 1 channel 3	Pod 1 channel 11	

3 Activate the data channels that are connected according to the previous table.

a In the Analyzer setup window, select the Format tab.

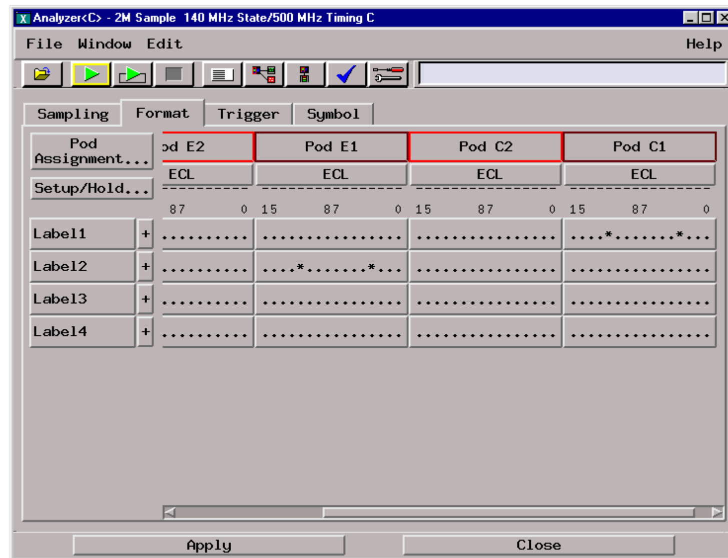
b Under the Format tab, select the field showing the channel assignments for Pod 1 of the Master card, then select Individual. Using the mouse, select channels 3 and 11. An asterisk means that a channel is turned on.

c For an Expander card, move the mouse cursor over the Label1 field, then click and hold the right mouse button. At the pop-up window, select Insert After. In the Enter Label Name field, enter “Label2”.

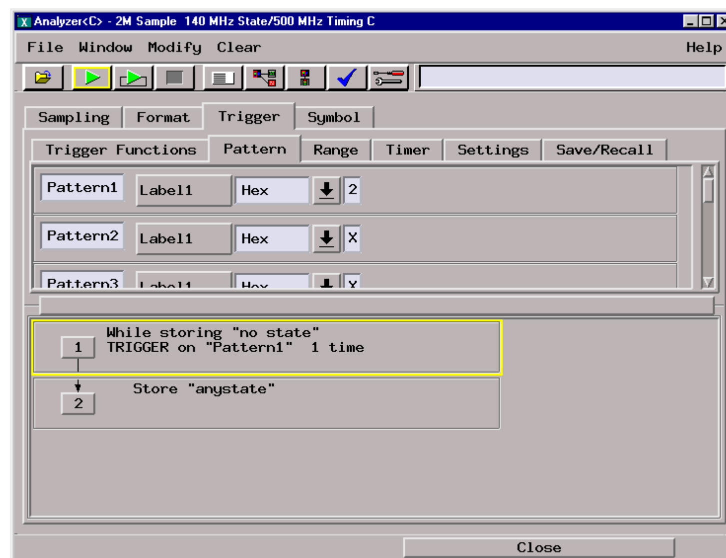
d Select the field showing the channel assignments in Label2 for Pod 1 of the Expander card. Select Individual, then select channels 3 and 11.

e Repeat steps c and d for a second Expander card, if installed. Enter “Label3” in the Label Name field and assign Pod 1 channels 3 and 11 of the Expander card to Label3.

f Repeat steps c and d for a third Expander card, if installed. Enter “Label4” in the Label Name field and assign Pod 1 channels 3 and 11 of the Expander card to Label4.



g Under the Trigger tab, select the Pattern tab. Select the pattern field associated with the “Pattern 1” pattern recognizer and enter “2”.



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 7.142 ns, +0 ps or -142 ps.

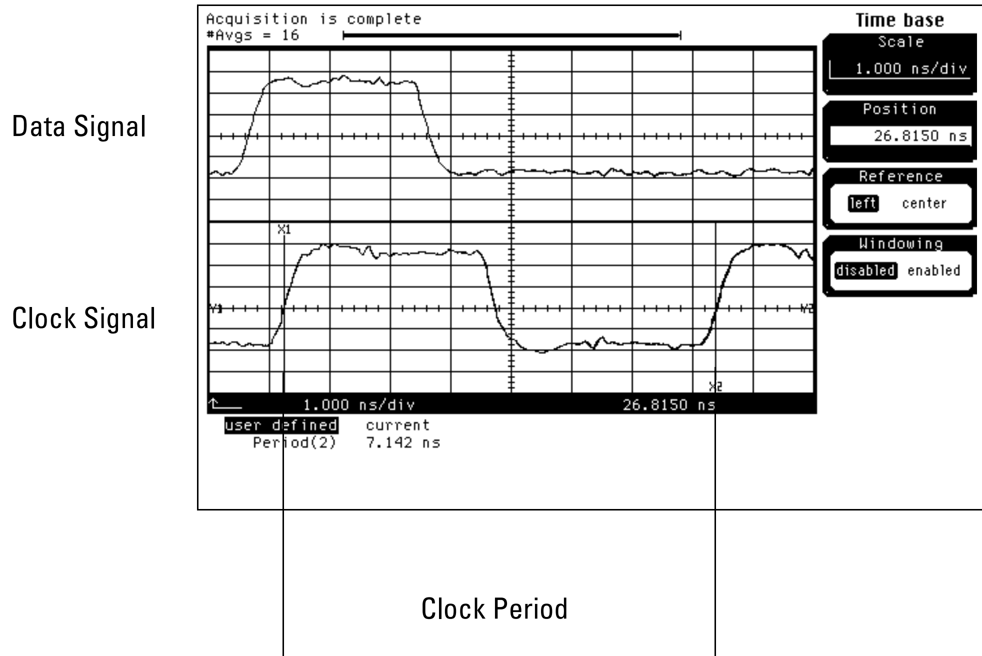
a Turn on the pulse generator channel 1, channel 2, and trigger outputs.

b In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

d On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 7.142 ns, go to step e. If the period is less than or equal to 7.142 ns but greater than 7.000 ns, go to step 2.

e In the oscilloscope Timebase menu, increase Position 7.142 ns. If the period is more than 7.142 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than or equal to 7.142 ns but greater than 7.000 ns.



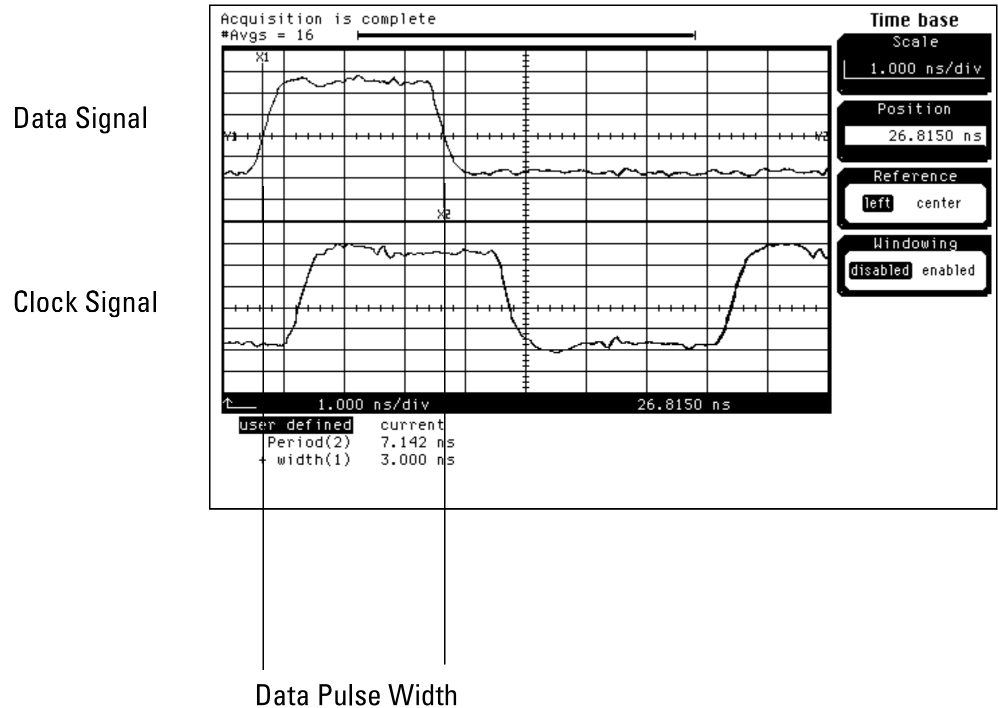
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.000 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



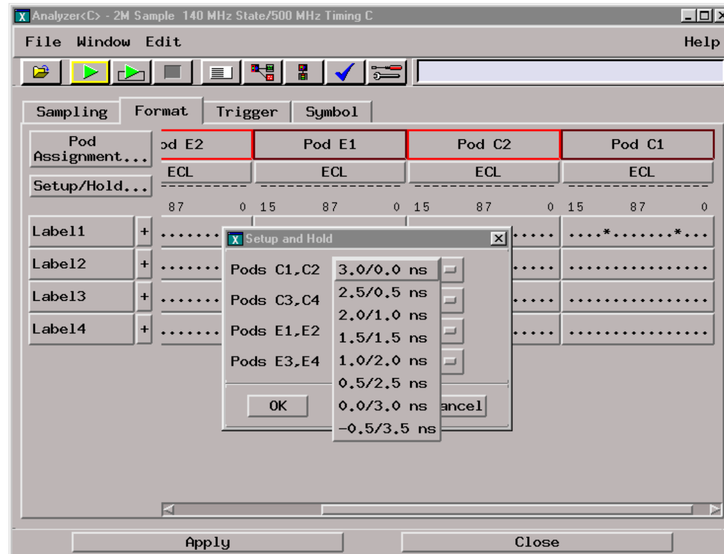
Check the setup/hold combination

1 Select the logic analyzer setup/hold time.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select Setup/Hold.

c In the Setup/Hold window, select the setup/hold field next to each Pod 1,2 pod pair, then select 3.0/0.0 ns. Repeat for all pods.



d Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

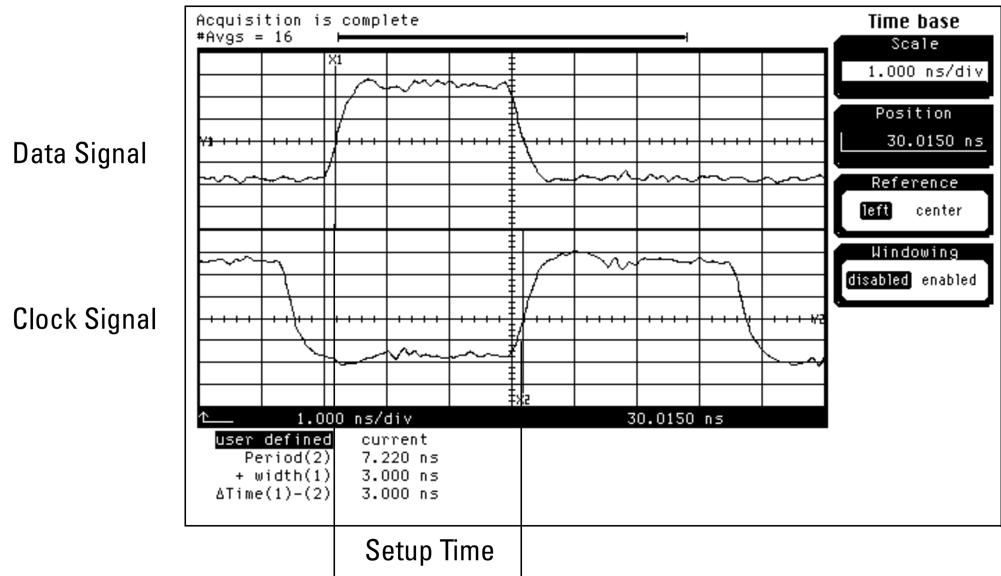
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the setup time is 3.000 ns, +0.0 ps or -100 ps.

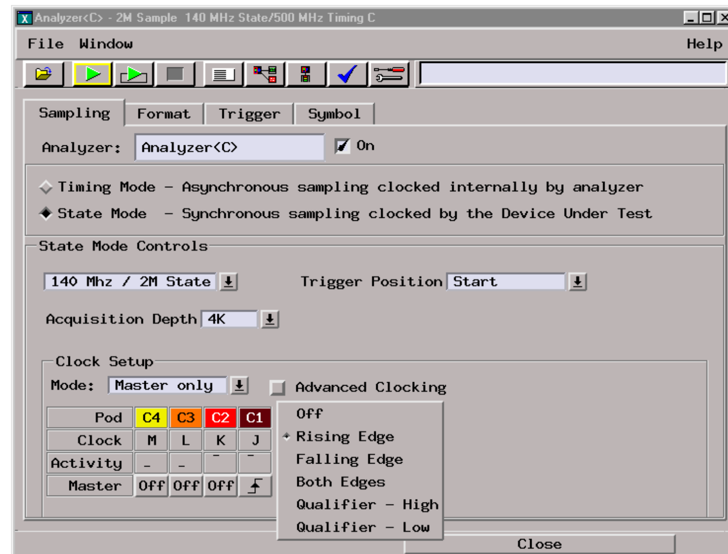


Disregard the Period(2) value. The settings provided in this procedure measure the period from falling edge to falling edge, which is not a valid measurement.

4 Select the clock to be tested.

a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select the close edge field under the clock to be tested. Ten select Rising Edge.



Clocks

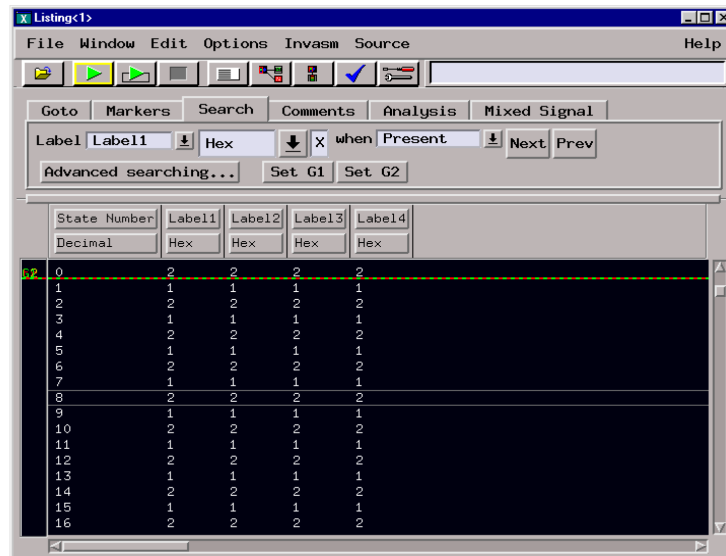
J↑	K↑	L↑	M↑

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

5 Configure the advanced searching.

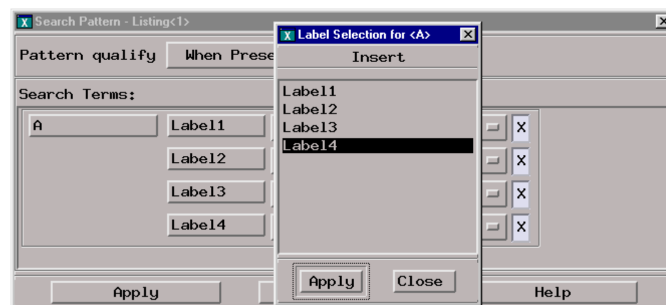
a In the Listing window, select the Run icon. The display should show an alternating pattern. The pattern depends on the number of cards.

Number of Cards	Alternating Pattern
four-card module	"2 2 2 2" and "1 1 1 1"
three-card module	"2 2 2" and "1 1 1"
two-card module	"2 2" and "1 1"



b In the Search Pattern window, select the Label1 button. At the pop-up menu, select Insert label, and the Insert window will appear.

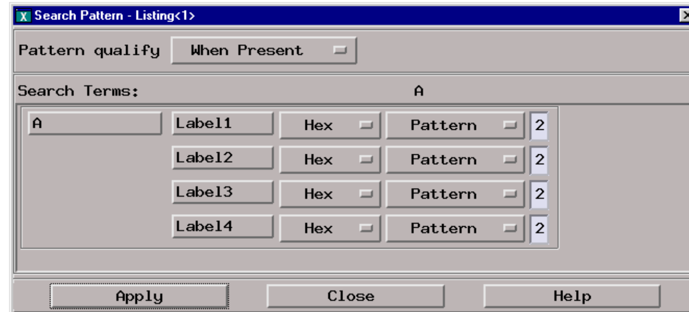
c In the Insert window, select "Label2", then Apply. Then select "Label3", then Apply. Then select "Label4", then Apply.



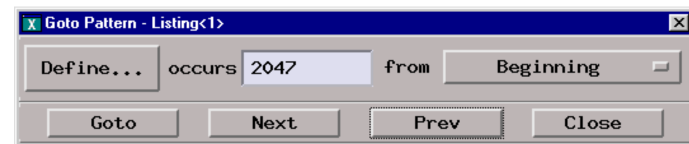
d Select Close to close the Insert window.

6 Verify the test data.

a In the Search Pattern window, enter “2” for Label1 and Label2, for Label3 (three-card module), and for Label4 (four-card module). Select Apply.



b In the Goto Pattern window, enter “2047” in the occurs field. Select the Goto button. If the “Pattern NOT Found” error message appears, the test fails.



c In the Search Pattern window, enter “1” for Label1 and Label2, for Label3 (three-card module), and for Label4 (four-card module). Select Apply.

d In the Goto Pattern window, enter “2048” in the occurs field. Select the Goto button. If the “Pattern NOT Found” error message appears, the test fails.

7 Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

To Test the Five-card Module

The five-card test is only required for configured five-card modules. Performing the test verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time

Five-card modules that were changed to one-card modules for the previous performance tests need to be reconfigured as a five-card module for this test.

This test checks a combination of data channels using a single-edge clock at one selected setup/hold time.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Pulse Generator	100 Mhz, 3.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)		8120-4948
Coupler (Qty 3)	BNC (m-m)	1250-0216
BNC Test Connector, 6x2 (Qty 3)		

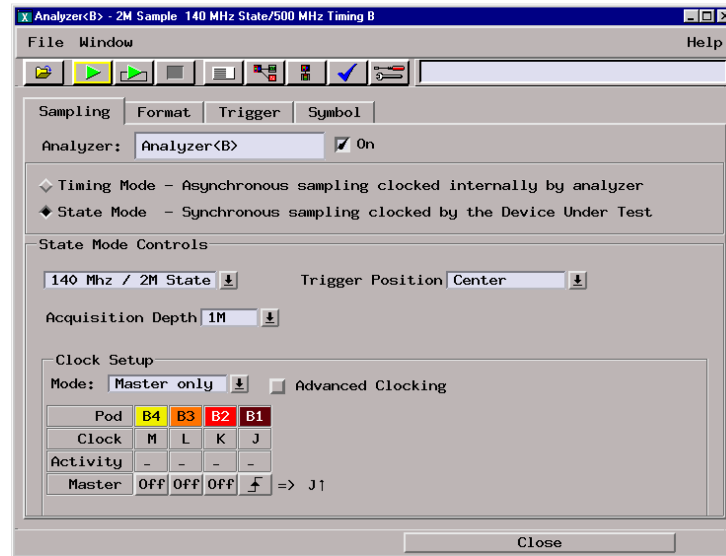
Set up the equipment

1. If you have not already done so, do the procedure “To Set up the Test Equipment and the Analyzer” on page 35. Ensure that the pulse generator and oscilloscope are set up according to the tables in that section.
2. Change the pulse generator Period to 10.000 ns.

Set up the logic analyzer

1. Set up the Sampling tab.
   a. In the Analyzer window, select the Sampling tab.
   b. Select State Mode.

c Select the 135MHz/2M state mode field, then select 140MHz/2M state.

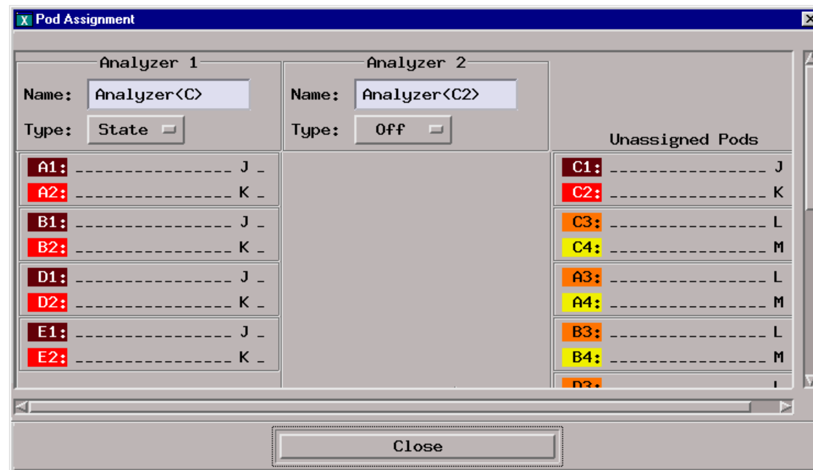


2 Assign pods 1 and 2 of all expander cards to Analyzer 1.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag pods1 and 2 to the Analyzer 1 column. Use the mouse to drag all pods 3 and 4 to the Unassigned Pods column.



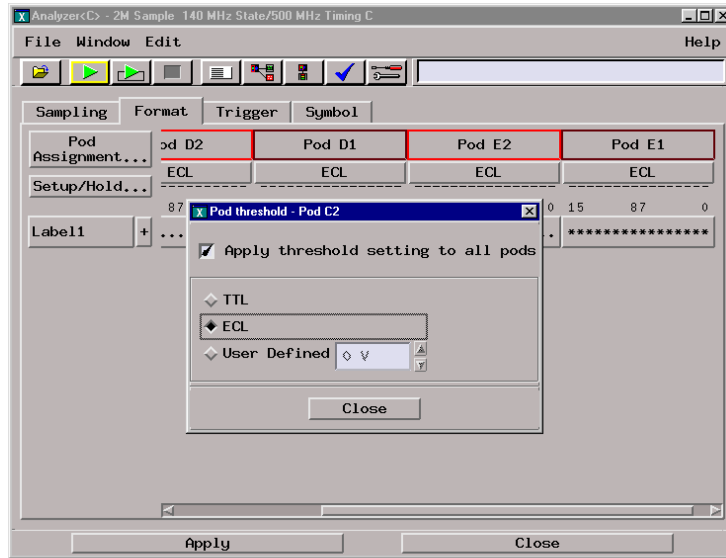
d Use the mouse to drag Pods C1, C2 (master card) to the Unassigned Pods column.

3 Set up the Format tab.

a Under one of the pod fields, select TTL.

b In the Pod Threshold window, ensure the Apply threshold settings to all pods checkbox is checked.

c In the Pod Threshold window, select ECL.



d Select Close to close the Pod Threshold window.

4 Set up the Trigger tab.

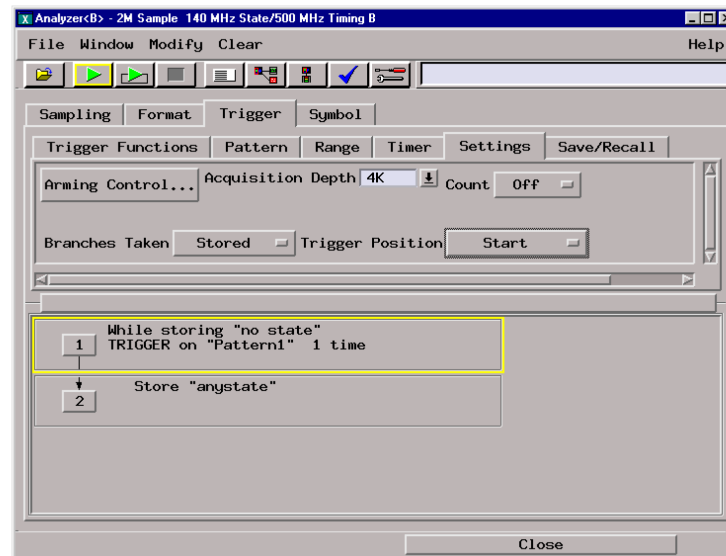
a In the Analyzer setup window, select the Trigger tab. Under the Trigger tab, select the Settings tab.

b Select the Acquisition Depth field, then select “4K”.

c Select the Count field, then select “Off”.

d Select the Trigger Position field, then select Start.

e Select the field labeled “1” in the Sequence field, then at the pop-up menu select Edit. In the pop-up window, select “anystate”, then select “no state”. Select Close to exit the sequence edit window.

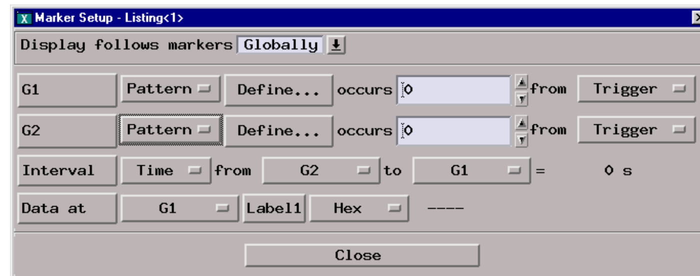


5 Set up the Listing window.

a In the Listing window, select the Markers tab.

b Select the G1: field and the Markers Setup window appears.

c Select the Time field associated with G1, and select Pattern. Select the Time field associated with G2, and select Pattern.

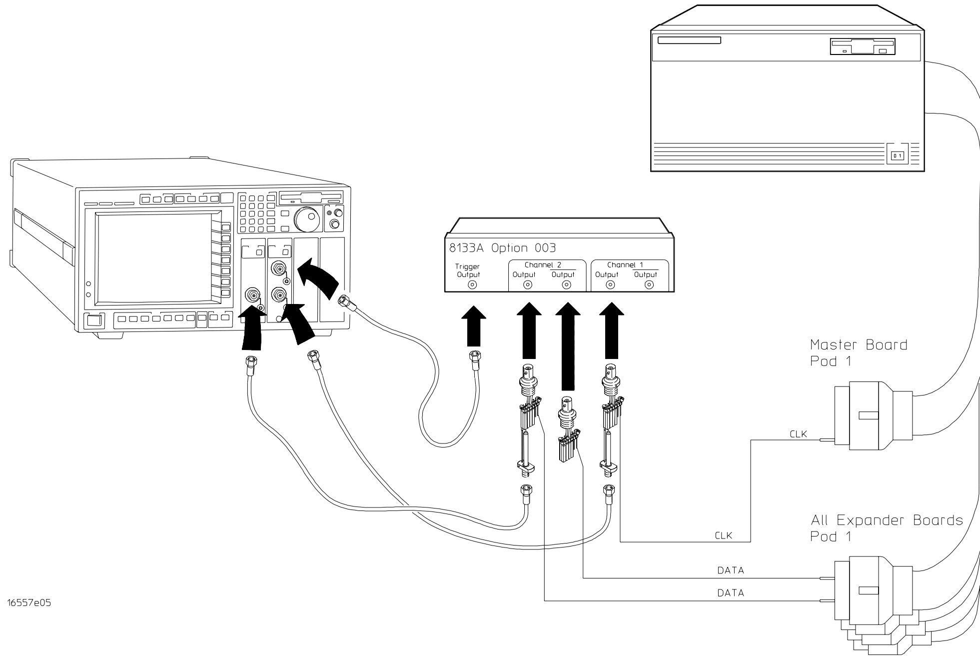


Note: Leave the Marker Setup window open. You will be entering numeric values in the "occurs" field after acquiring the test data.

Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the logic analyzer clock and data channels listed in the following tables to the pulse generator.

2 Using SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator according to the following illustration.



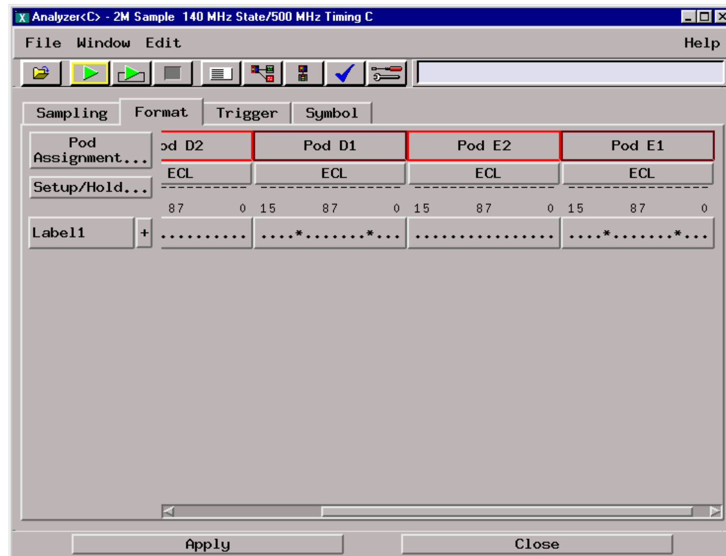
Connect the 16557D to the Pulse Generator

Agilent 8133A Ch2 Output	8133A Ch2 $\overline{\text{Output}}$	8133A Ch1 Output
All Expander cards, Pod 1 channel 3	All Expander cards, Pod 1 channel 11	Master card J-clock

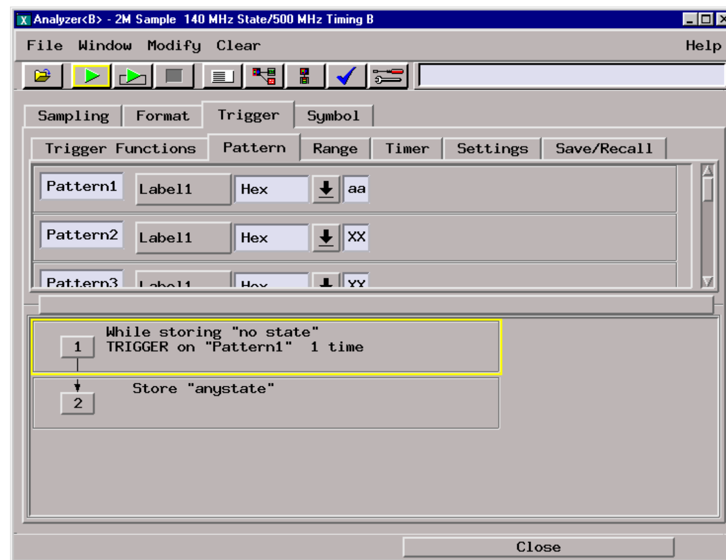
3 Activate the data channels that are connected according to the previous table.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select the field showing the channel assignments for Pod 1 of one of the Expander cards, then select Individual. Using the mouse, select channels 3 and 11. An asterisk means that a channel is turned on. Follow this step for the Pod 1 of each of the remaining Expander cards.



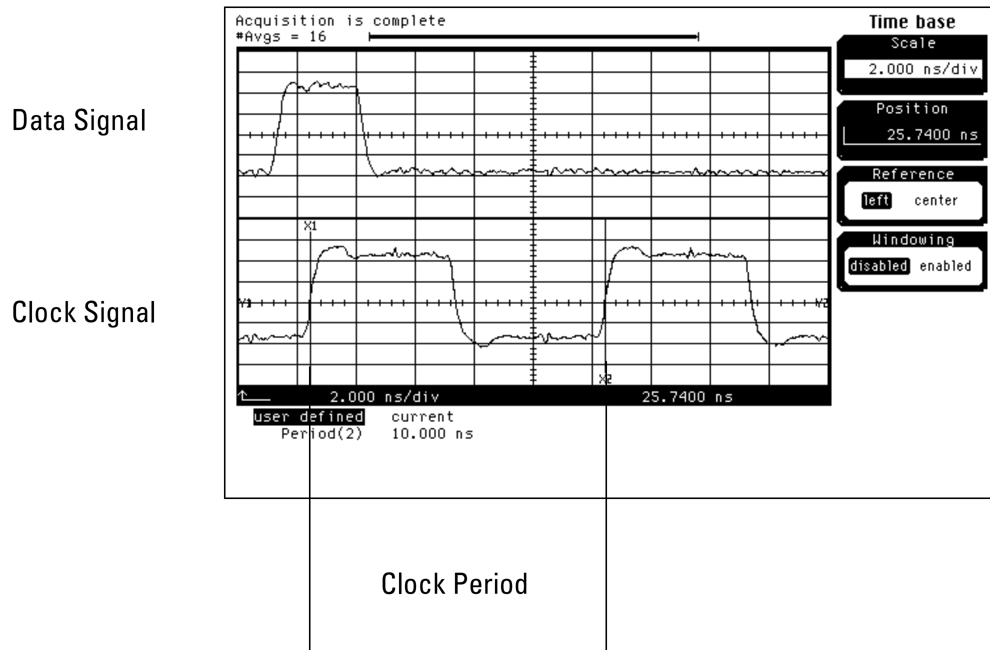
c Under the Trigger tab, select the Pattern tab. Under the Pattern tab, select the pattern field associated with pattern recognizer "Pattern1". Enter "aa".



Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

- **a** Turn on the pulse generator channel 1, channel 2, and trigger outputs.
- **b** In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **d** On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is more than 10.000 ns, go to step e. If the period is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.
- **e** In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is more than 10.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than or equal to 10.000 ns but greater than 9.750 ns.



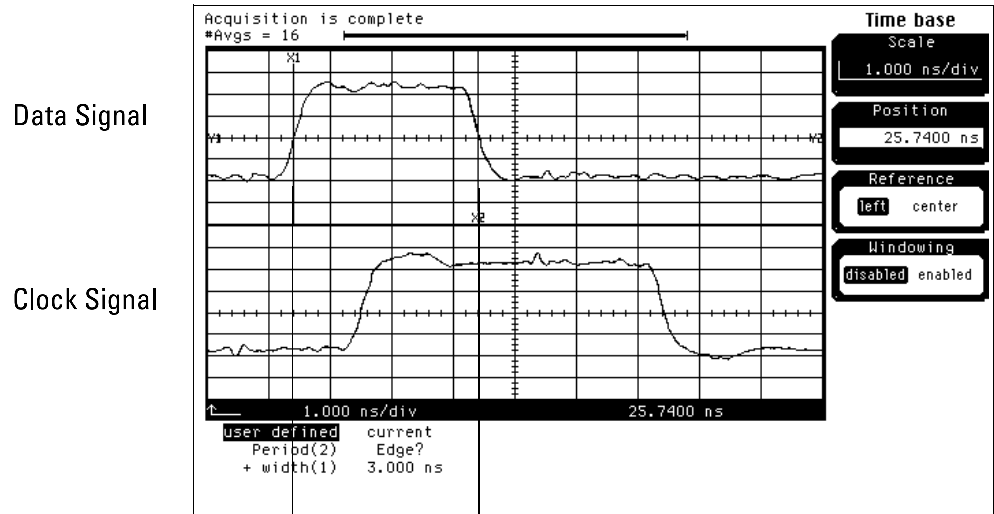
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.000 ns, +0 ps or -100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Data Pulse Width

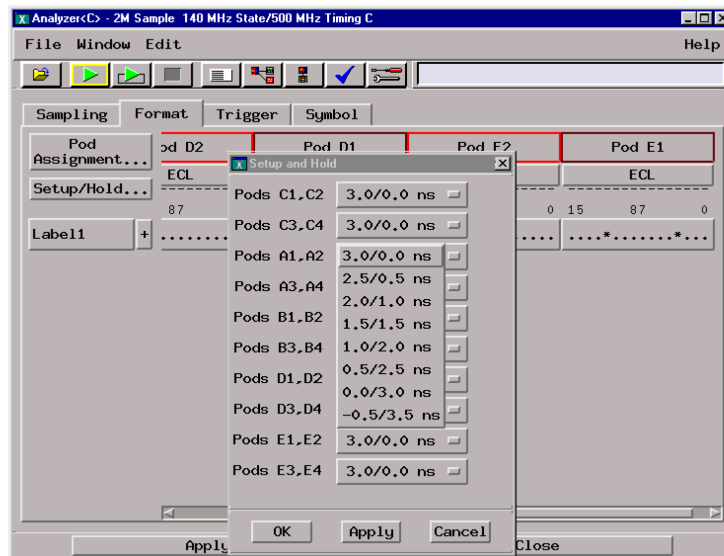
Check the setup/hold combination

1 Select the logic analyzer setup/hold time.

a In the Analyzer setup window, select the Format tab.

b Under the Format tab, select Setup/Hold.

c In the Setup/Hold window, select the setup/hold field next to each Pod 1, 2 pod pair, then select 3.0/0.0 ns. Repeat for all pods.



d Select OK to exit the Setup/Hold window.

2 Disable the pulse generator channel 1 COMP (LED off).

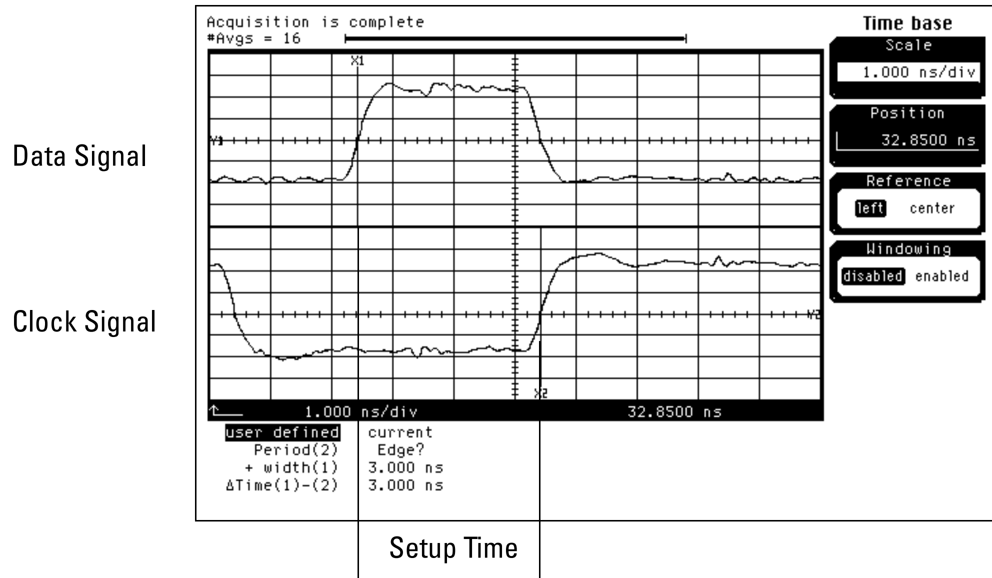
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define ΔTime - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position both a clock and a data waveform on the display, with the rising edge of the clock waveform centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (ΔTime(1)-(2)).

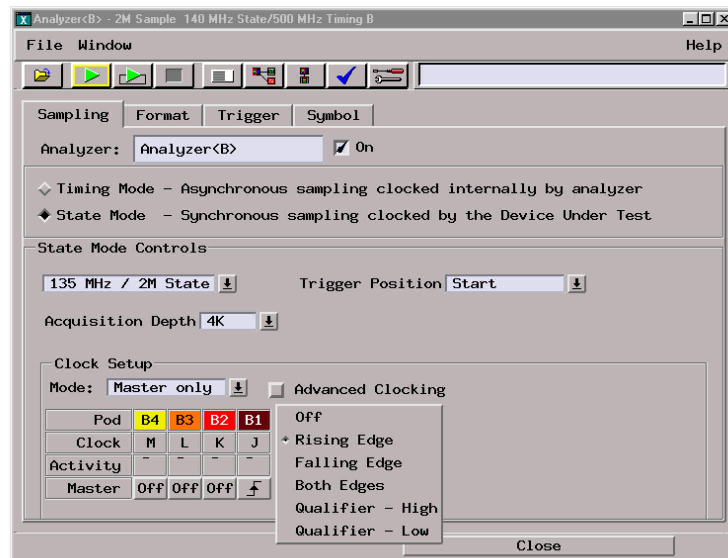
d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



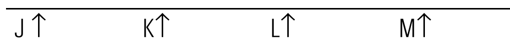
4 Select the clock to be tested.

a In the Analyzer setup window, select the Sampling tab.

b Under the Sampling tab, select the clock edge field under the clock to be tested. Then select Rising Edge.



Clocks

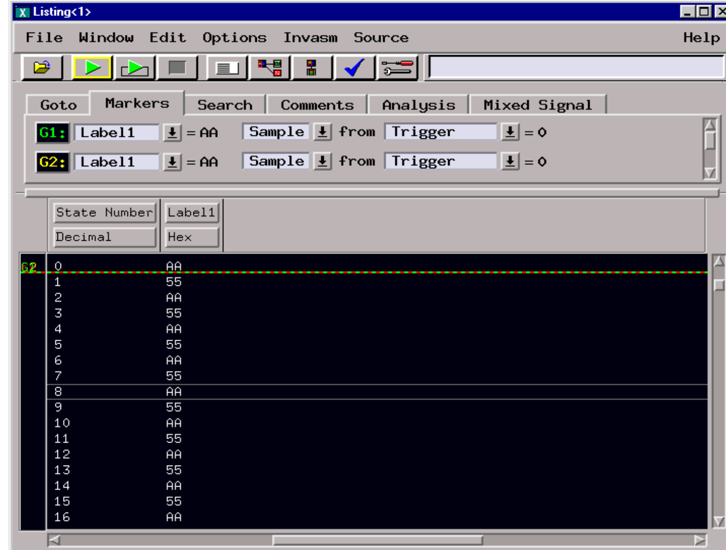


J↑	K↑	L↑	M↑

c Connect the clock input channel to be tested to the pulse generator channel 1 OUTPUT. Disconnect all other clock input channels.

5 Verify the test data.

a In the Listing window, select the Run icon. The display should show an alternating pattern of “AA” and “55”.

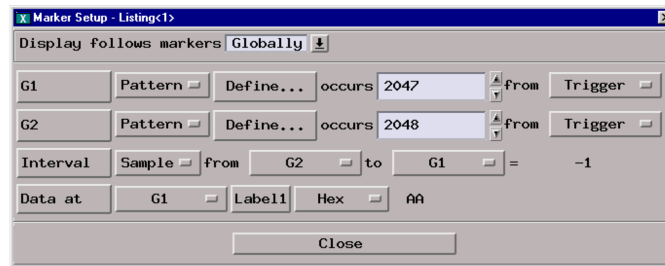


b In the Marker Setup window, select the Define... field associated with G1, and the G1 Marker Pattern window appears. In the pattern field, enter “aa”. Select Apply, then select Close.

c In the Marker Setup window, select the Define... field associated with G2, and the G2 Marker Pattern window appears. In the pattern field, enter “55”. Select Apply, then select Close.

d In the Marker Setup window, select the ‘occurs’ value field that corresponds to marker G1. Enter 2047.

e In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 2048.



f Select Close to apply the marker values to the data. If the "Pattern NOT found for marker…" error message does not appear, then the test passes. Record the Pass or Fail in the performance test record.

6 Repeat steps 4, 5, and 6 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

Performance Test Record

Performance Test Record

Agilent Technologies 16557D Logic Analyzer	
Serial No. ________________________	Work Order No.____________________
Recommended Test Interval - 2 Year/4000 hours	Date____________________________
Recommended next testing_______________	Temperature______________________

Test	**Settings**		**Results**	
Self-Tests			Pass/Fail	________
Threshold Accuracy	±(100 mV + 3% of threshold setting)			
Pod 1			Limits	Measured
	ECL, ±139 mV	ECL VL	−1.439 V	________
		ECL VH	−1.161 V	________
	0 V, ±100 mV	0 V User VL	−100 mV	________
		0 V User VH	+100 mV	________
Pod 2				
	ECL, ±139 mV	ECL VL	−1.439 V	________
		ECL VH	−1.161 V	________
	0 V, ±100 mV	0 V User VL	−100 mV	________
		0 V User VH	+100 mV	________
Pod 3				
	ECL, ±139 mV	ECL VL	−1.439 V	________
		ECL VH	−1.161 V	________
	0 V, ±100 mV	0 V User VL	−100 mV	________
		0 V User VH	+100 mV	________
Pod 4				
	ECL, ±139 mV	ECL VL	−1.439 V	________
		ECL VH	−1.161 V	________
	0 V, ±100 mV	0 V User VL	−100 mV	________
		0 V User VH	+100 mV	________

Test	**Settings**		**Results**	
Single-Clock, Single-Edge Acquisition				
All Pods	Setup/Hold Time	3.0/0.0 ns	J↑	_________
			K↑	_________
			L↑	_________
			M↑	_________
			J↓	_________
			K↓	_________
			L↓	_________
			M↓	_________
	Setup/Hold Time	-0.5/3.5 ns	J↑	_________
			K↑	_________
			L↑	_________
			M↑	_________
			J↓	_________
			K↓	_________
			L↓	_________
			M↓	_________

Test	Settings		Results			
Multiple-clock, Multiple-edge acquisition				Pass/Fail		Pass/Fail
All Pods	Setup/Hold Time	4.0/0.0 ns	J↑+ K↑+L↑ + M↑	________	J↓+ K↓+L↓+ M↓	________
	Setup/Hold Time	-0.5/4.5 ns	J↑+ K↑+L↑+ M↑	________	J↓+ K↓+L↓+ M↓	________
Single-Clock, Multiple-Edge Acquisition				Pass/Fail		
All Pods	Setup/Hold Time	3.5/0.0 ns	J↕	________		
			K↕	________		
			L↕	________		
			M↕	________		
	Setup/Hold Time	-0.5/4.0 ns	J↕	________		
			K↕	________		
			L↕	________		
			M↕	________		
Time Interval Accuracy				Pass/Fail		
	Interval time from G1 to G2	749.921 - 750.079 µs		________		
Multi-Card Test				Pass/Fail		
	Setup/Hold Time	3.0/0.0 ns	J↑	________		
			K↑	________		
			L↑	________		
			M↑	________		

4

Calibrating

Calibration Strategy

The 16557D logic analyzer does not require an operational accuracy calibration. To test the module against the module specifications, refer to "Testing Performance" in chapter 3.

5

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Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, a cable test, and a test for the auxiliary power supplied by the probe cable. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.

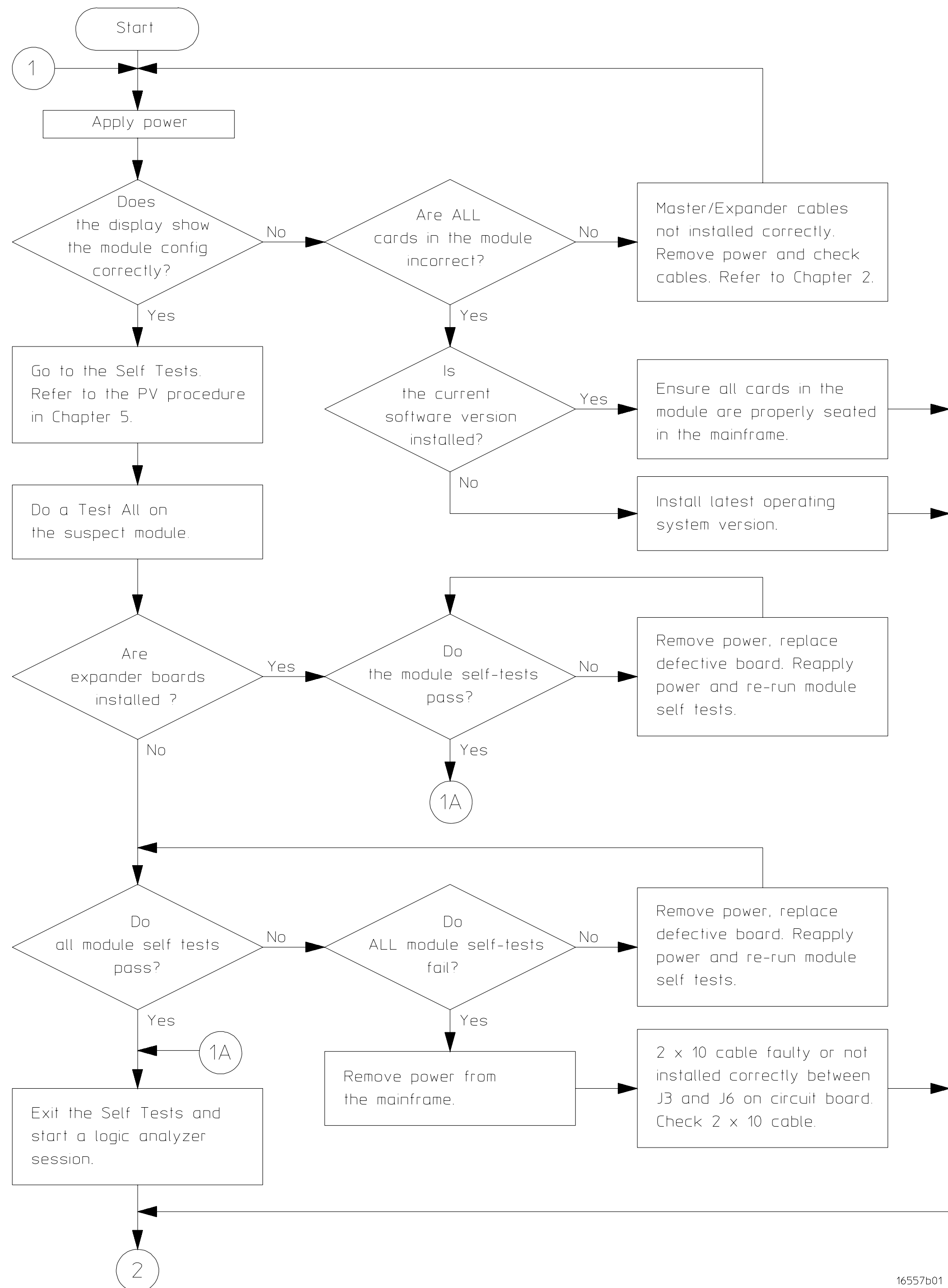
To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.

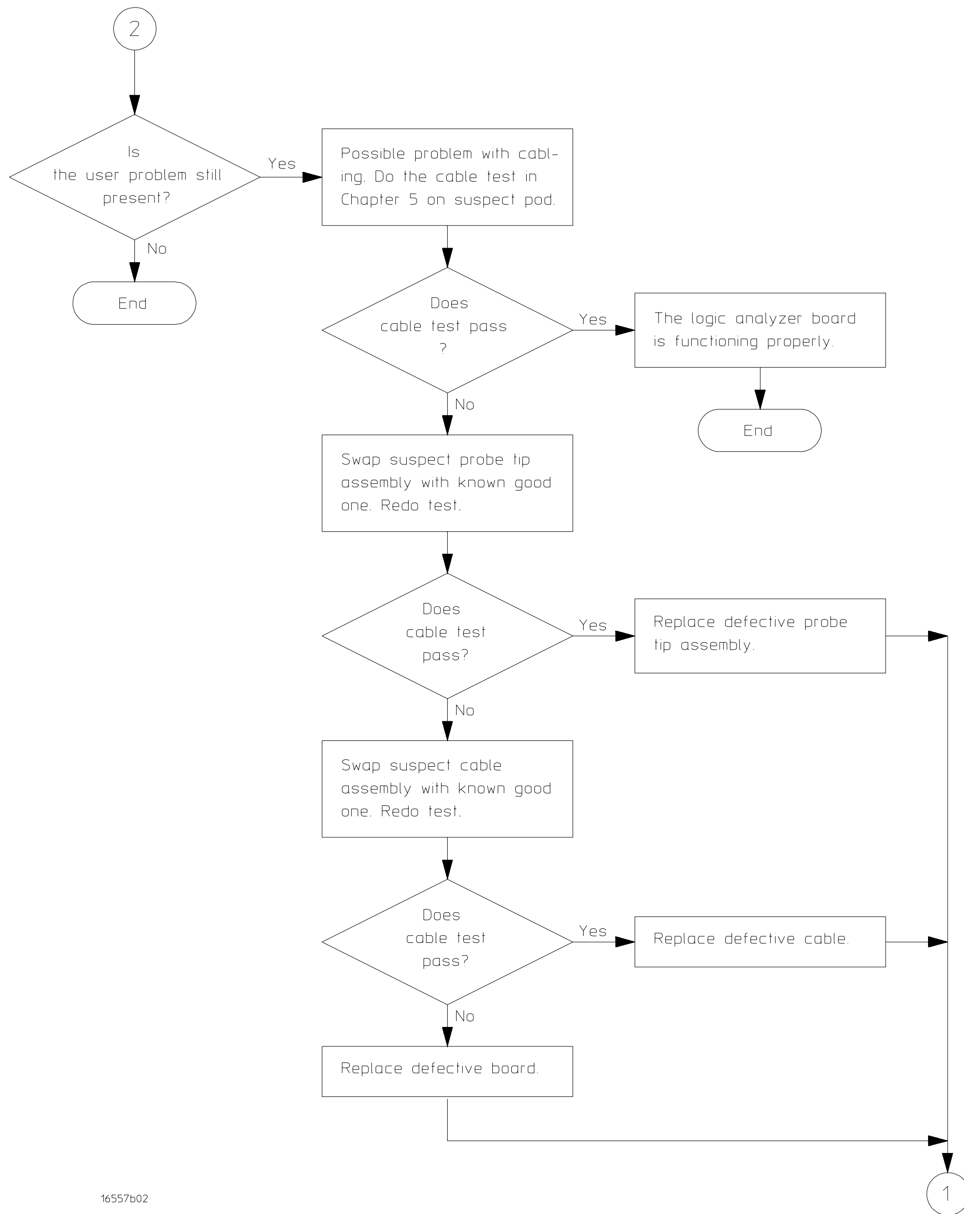
Mainframe Operating System

Before starting the troubleshooting on an 16557D, ensure that the required version of Agilent Technologies 16700-series mainframe operating system is installed on the mainframe. The required operating system software versions are listed in "Mainframe and Operating System" in chapter 1. To check the operating system version number, open the System Administration window, click the Admin tab, then click About...

If the proper version is not loaded, obtain a copy of the updated operating system software and install it in the logic analyzer.



Troubleshooting Flowchart 1



Troubleshooting Flowchart 2

To run the self-tests

Self-tests identify the correct operation of major, functional subsystems of the module. You can run all self-tests without accessing the module. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the module.

To run the self-tests:

1 In the System window, select System Admin.

2 In the System Administration window, select the Admin tab, then select Self-Test. At the Test Query window, select Yes.

The tests can be run individually, or all the tests can be run by selecting Test All at the bottom of the Self Test window. Note that if Test All is selected, system tests requiring user action will not be run. For more information, refer to Chapter 8 in the mainframe service manual.

3 In the Self Test window under the System tab, select System CPU Board.

4 Run the floppy drive test.

a In the Self Test: System CPU Board window, select Floppy Drive Test.

b Insert a DOS-formatted disk with 300KB of available space in the mainframe floppy drive.

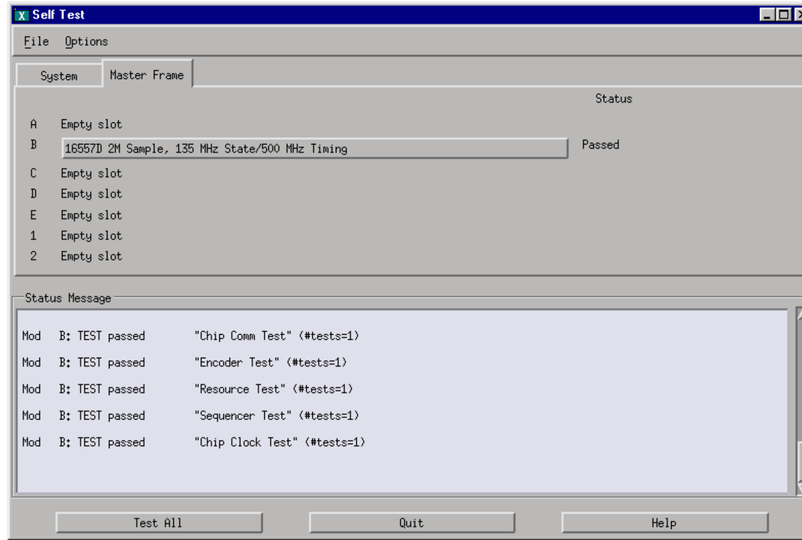
c In the Test Query window, select OK.

The Test Query window instructs you to insert the disk into the disk drive. The other System CPU Board tests require similar user action to successfully run the test.

5 In the Self Test: System CPU Board window, select Close to close the window.

6 In the Self Test window, select PCI Board. Select Test All to run all PCI board tests.

7 In the Self Test window, select the Master Frame tab. Select the 16557D module to be tested, then select Test All to run all the module tests. The module test status should indicate PASSED (see screen on next page).



Refer to Chapter 8 in the mainframe service manual for more information on system tests that are not executed.

To exit the test system

To exit the test system

1. Select Close to close any module or system test windows.
2. In the Self Test window, select Quit.
3. In the session manager window, select Start Session on This Display to launch a new logic analyzer session.

To test the cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Agilent Model/Part
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	8133A Option 003
6x2 Test Connectors (Qty 4)		

1 If you have not already done so, do the procedure "To set up the test equipment and the logic analyzer" in Chapter 3.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table

Pulse Generator Setup

Timebase	Channel 2	Channel 1	Trigger
Mode: Int Period: 25.000 ns	Mode: Square Delay: 0.000 ns High: 3.00 V Low: 0.00 V COMP: Disabled (LED Off)	Mode: Square Delay: 0.000 ns High: 3.00 V Low: 0.00 V COMP: Disabled (LED Off)	Divide: Divide ÷ 1 Ampl: 0.50 V Offs: 0.00 V

b Enable the pulse generator channel 1 and channel 2 outputs (LED off).

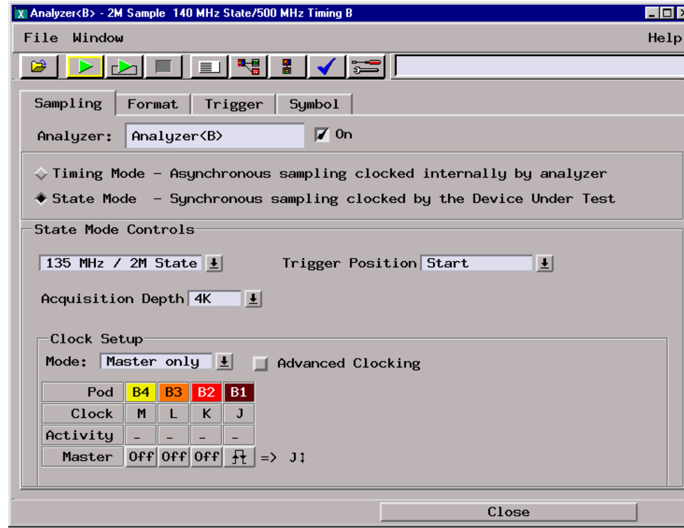
3 Set up the Sampling tab.

a In the Analyzer window, select the Sampling tab.

b Select State Mode.

c Select Master Clock. In the Master Clock window, select both edges for the J clock (J↑). Turn off the other clocks.

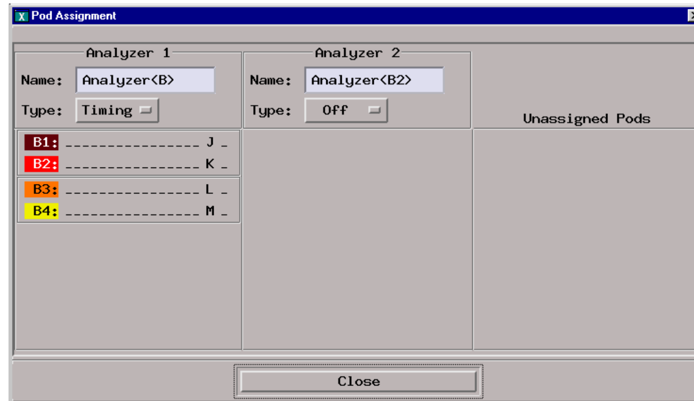
d Select Acquisition Depth field, then select 4K.



4 Assign all pods to Analyzer 1, and configure the pod under test.

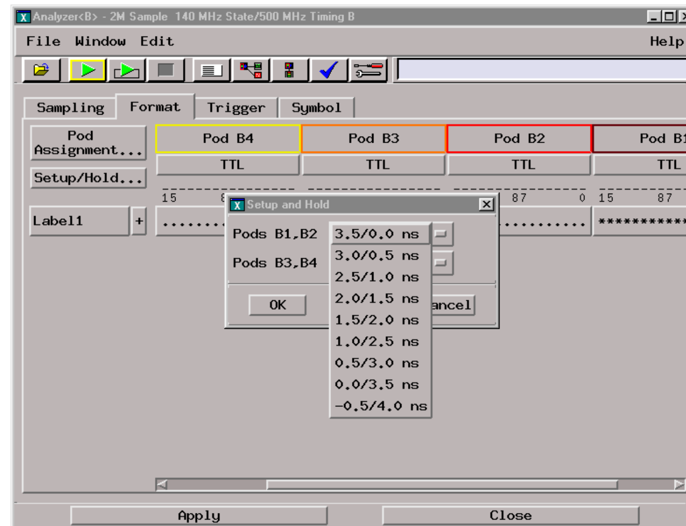
a Select the Format tab. Under the Format tab, select Pod Assignment.

b Use the mouse to drag the pods to the Analyzer column.



c Select the field showing the channel assignments for the pod under test. In the pop-up menu, select the asterisk field to put asterisks in the channel positions, activating the channels. Select Done.

d Select Setup/Hold field for the pod under test, then select 3.5/0.0 ns. Select Ok to close the Setup/Hold window.

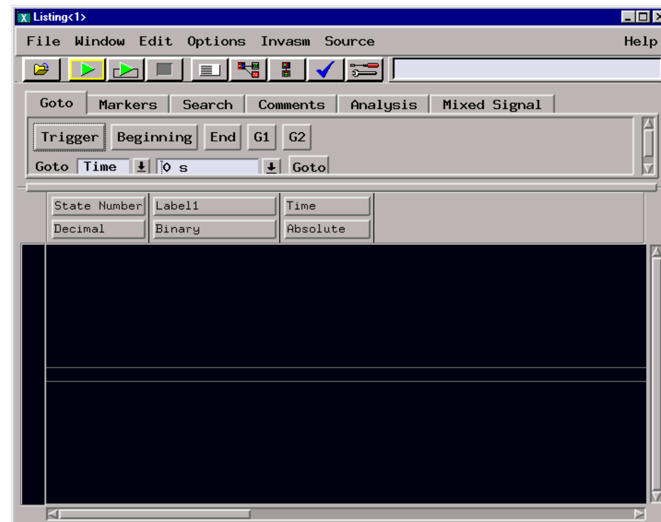


e Ensure the threshold is set to TTL. If not, select the threshold field, then select TTL.

5 Set up the Listing window.

a In the Analyzer Setup window, select Window, then select Slot n: Analyzer (where “n” is the slot the module under test is installed), then select Listing. A Listing window opens.

b Right click on the Hex field and change the Label1 base to Binary.



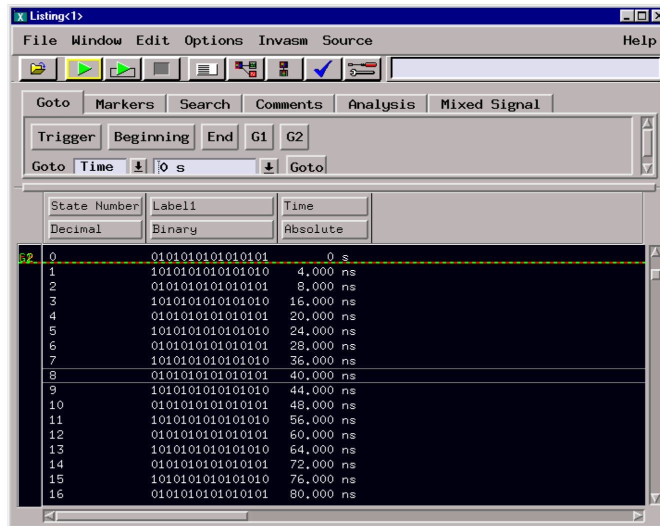
6 Using four 6-by-2 test connectors, connect the logic analyzer to the pulse generator channel outputs. To make the test connectors, see chapter 3, “Testing Performance”.

a Connect the even-numbered channel of the lower byte of pod under test to the pulse generator channel 1 Output.

b Connect the odd-numbered channel of the lower byte of the pod under test to the pulse generator channel 1 Output.

- **c** Connect the even-numbered channel of the upper byte of the pod under test and the J clock channel to the pulse generator channel 2 Output. J clock is located on Pod 1.
- **d** Connect the odd-numbered channel of the upper byte of the pod under test to the pulse generator channel 2 Ouput.

7 On the logic analyzer, select the Run icon. The listing should look similar to the figure below. Ignore any error messages dealing with G1 and G2 markers.



8 If the listing looks like the figure, then the cable passed the test.

If the listing does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for the cable test failures include:

- open channel.
- channel shorted to a neighboring channel.
- channel shorted to either ground or a supply voltage.

Return to the troubleshooting figure.

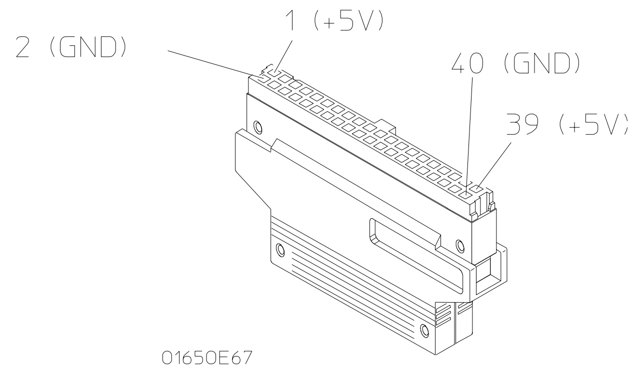
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection circuit. If the current on pins 1 and 39 exceeds 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Agilent Model/Part
Digital Multimeter	na	E2373A

- Using the multimeter, verify the +5 V on pins 1 and 39 of the probe cables.



6

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To replace the circuit board 134

To replace the module 135

To replace the probe cable 137

To replace the Reference Clock cable 138

To return assemblies 139

Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module. Also in this chapter are instructions for returning assemblies.

CAUTION Turn off the instrument before installing, removing, or replacing a module in the instrument.

Tools Required

- A T10 TORX screwdriver, to remove screws connecting the probe cables and screws connecting the back panel.
- A 1/4-inch hollow-shaft nutdriver, to remove the nut holding the cable to the module panel insert.

To remove the module

CAUTION

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

1 Remove power from the instrument.

a Exit all logic analysis sessions. In the session manager, select Shutdown.

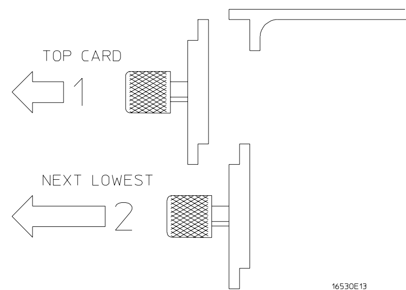
b At the query, select Power Down.

c When the "OK to power down" message appears, turn the instrument off.

d Disconnect the power cord.

2 Loosen the thumb screws.

Starting from the top, loosen the thumb screws on the filler panels and cards located above the module and the thumb screws of the module.



3 Starting from the top, pull the cards and filler panels located above the module half-way out.

4 If the module consists of a single card, pull the card completely out.

If the module consists of multiple cards, pull all cards completely out.

5 Push all other cards into the card cage, but not completely in.

This is to get them out of the way for removing and replacing the module.

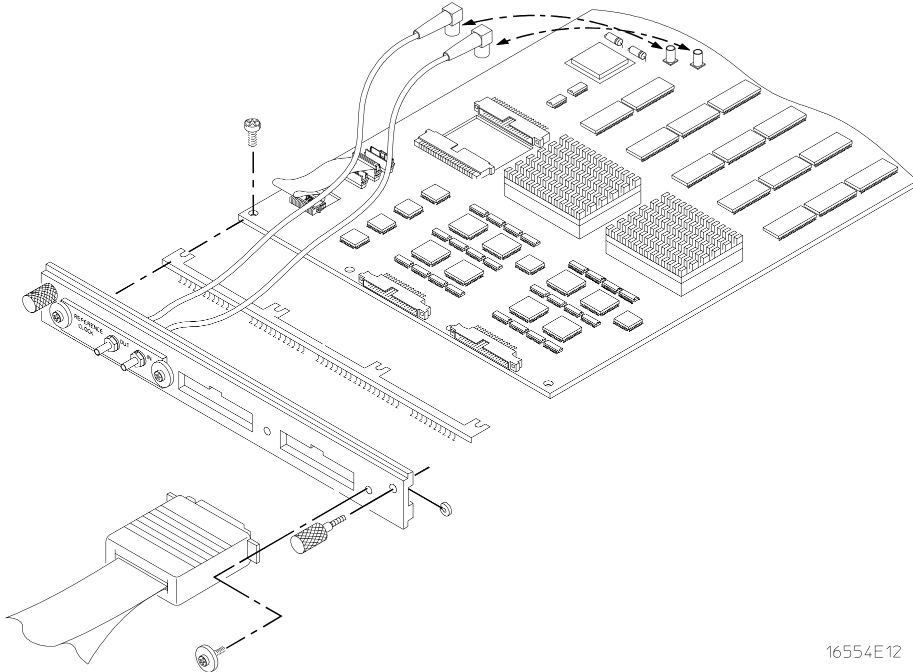
6 If the module consist of a single card, replace the faulty card.

If the module consists of multiple cards, remove the cables from J9 and J10 of all cards. Remove the 2x10 cables from J4, J5, J7, and J8 from the master card. Remove the faulty card from the module.

To replace the circuit board

1. Remove the three screws connecting the probe cables to the back panel, then disconnect the probe cables.
2. Remove the Reference Clock cables from connectors J12 and J13 on the circuit board.
3. Remove the four screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.
4. Replace the faulty circuit board with a new circuit board. On the faulty board, make sure the 20-pin ribbon cable is connected between J3 and J6.
5. Position the ground spring and back panel on the back edge of the replacement circuit board. Install four screws to connect the back panel and ground spring to the circuit board.
6. Connect the Reference Clock In cable to connector J13 on the circuit board. Connect the Reference Clock Out cable to J12 on the circuit board.
7. Connect the probe cables, then install three screws to connect the cables to the back panel.

CAUTION If you over tighten the screws, the threaded inserts on the back panel might break off of the back panel. Tighten the screws only enough to hold the cable in place.



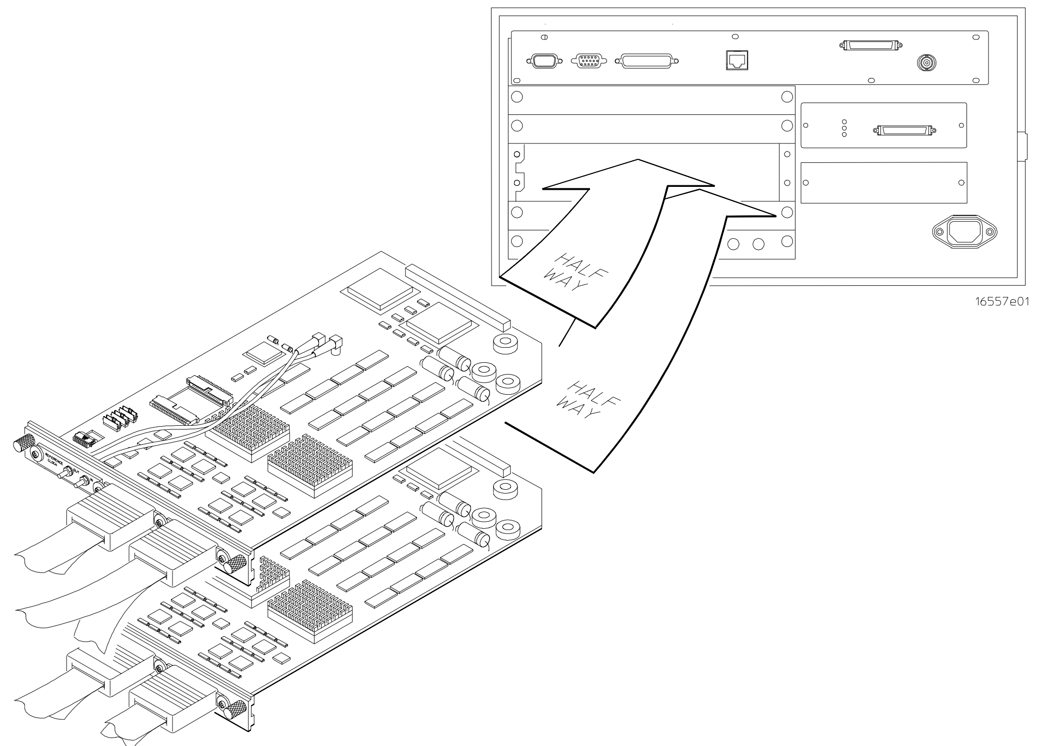
To replace the module

1 If the module consists of one card, go to step 2.

If the module consists of more than one card, connect the cables together in a master/expander configuration. Follow the procedure "To configure a multicard module" in chapter 2.

2 Slide the cards above the slots for the module about halfway out of the mainframe.

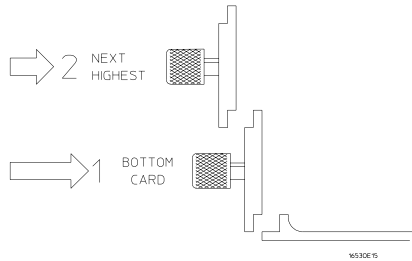
3 With the probe cables facing away from the instrument, slide the module approximately halfway into the mainframe.



4 Slide the complete module into the mainframe, but not completely in.

Each card in the instrument is firmly seated and tightened one at a time in step 6.

5 Position all cards and filler panels so that the endplates overlap.



6 Seat the cards and tighten the thumbscrews.

Starting with the bottom card, firmly seat the cards into the backplane connector of the mainframe. Keep applying pressure to the center of the card endplate while tightening the thumbscrews finger-tight. Repeat this for all cards and filler panels starting at the bottom and moving to the top.

CAUTION Correct air circulation keeps the instrument from overheating. For correct air circulation, filler panels must be installed in all unused card slots. Keep any extra filler panels for future use.

To replace the probe cable

1 Remove power from the instrument.

a Exit all logic analysis sessions. In the session manager, select Shutdown.

b At the query, select Power Down.

c When the “OK to power down” message appears, turn the instrument off.

d Disconnect the power cord.

2 Remove the screws that hold the probe cable to the rear panel of the module.

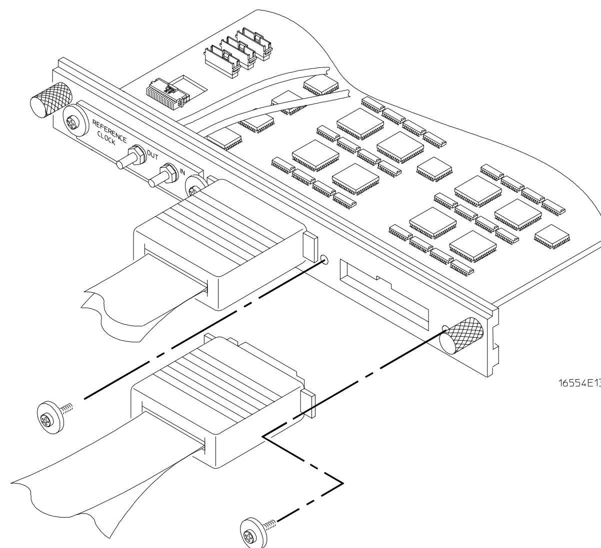
3 Remove the faulty probe cable from the connector and install the replacement cable.

4 Install the label on the new probe.

If you order a new probe cable, you will need to order new labels. Probe cables shipped with the module are labeled. Probe cables shipped separately are not labeled. Refer to chapter 7, "Replaceable Parts," for the part numbers and ordering information.

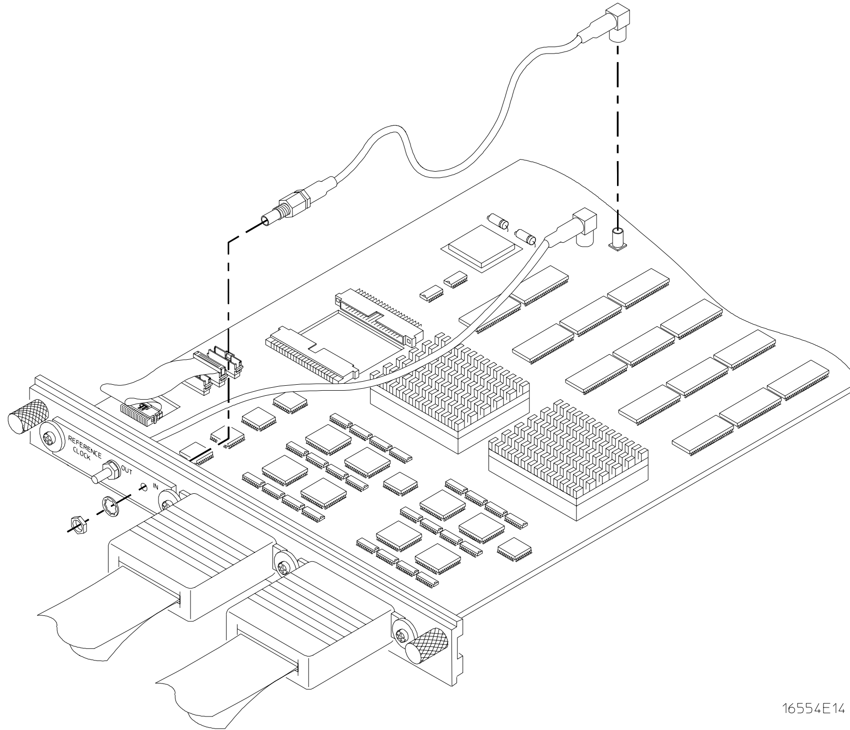
5 Install the screws connecting the probe cable to the rear panel of the module.

CAUTION If you over tighten the screws, the threaded inserts on the back panel might break off of the back panel. Tighten the screws only enough to hold the cable in place.



To replace the Reference Clock cable

1. Remove the module from the mainframe. Follow the procedure “To remove the module” on page 133.
2. Unplug the faulty Reference Clock cable from the circuit board REF CLK OUT (J12) or REF CLK IN (J13) connector.
3. Using a 1/4 inch hollow shaft nutdriver, remove the nut that holds the cable to the module panel insert.
4. Remove and replace the faulty Reference Clock cable. Insert the connector nut and gently tighten the nut using the nutdriver.
5. Plug the replacement cable into the board REF CLK OUT (J12) or REF CLK IN (J13). connector.
6. Follow the procedure "To replace the module" to reinstall the module into the mainframe.



To return assemblies

Before shipping the module to Agilent Technologies, contact your nearest Agilent Technologies Sales Office for additional details. In the U.S., call 1-800-403-0801.

1 **Write the following information on a tag and attach it to the module.**

- Name and address of owner
- Model number
- Serial number
- Description of service required or failure indications

2 **Remove accessories from the module.**

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 **Package the module.**

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION For protection against electrostatic discharge, package the module in electrostatic material.

4 **Seal the shipping container securely, and mark it FRAGILE.**

7

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Exploded View 145

Replaceable Parts

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies Sales Office.

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

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Exchange Assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies Sales Office for information.

See Also

To return assemblies 139

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

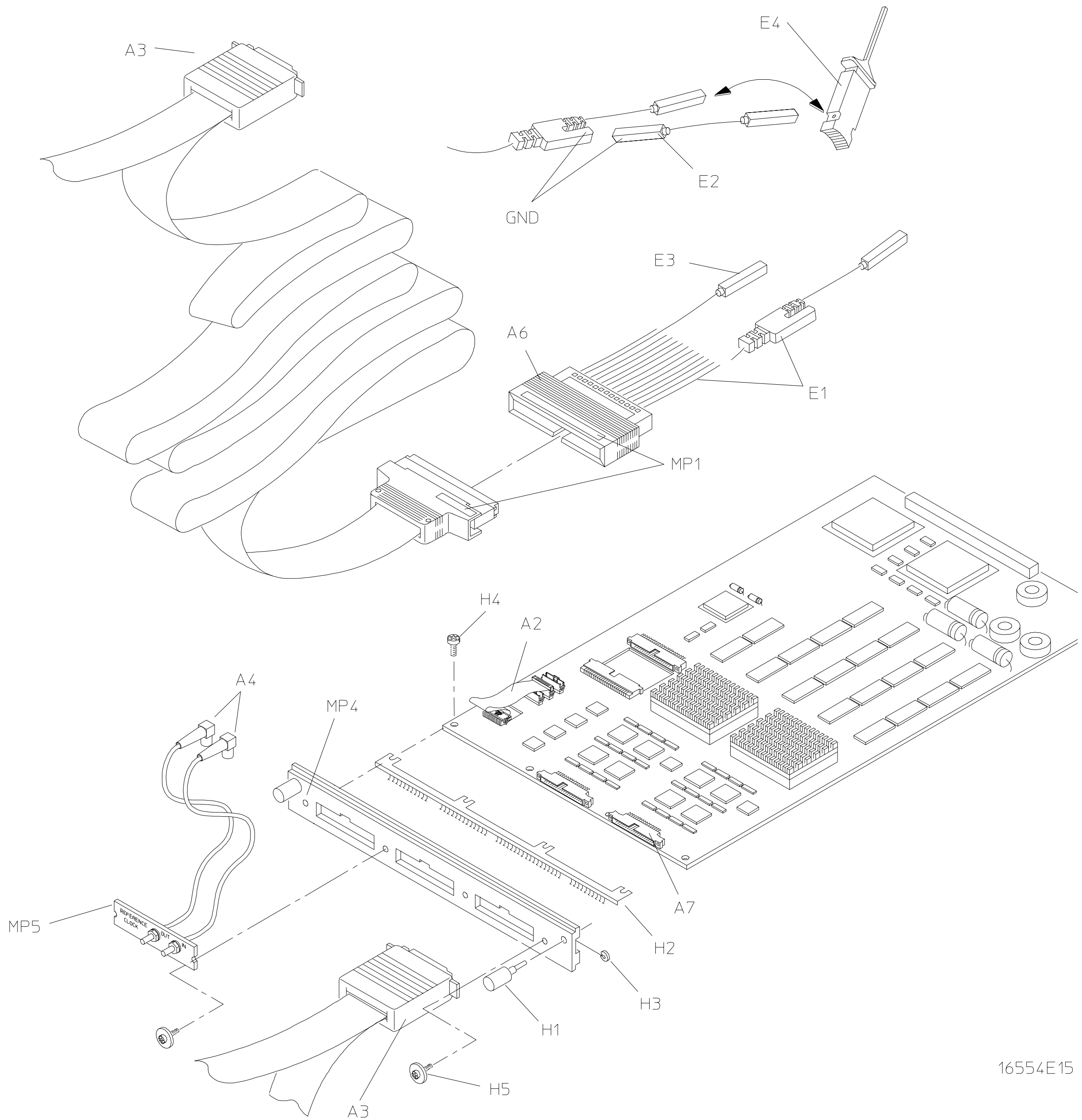
- Reference designator
- Agilent Technologies part number
- Total quantity included with the module (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- H Hardware
- J Connector
- MP Mechanical Part
- W Cable

Replaceable Parts			
Ref. Des.	**Agilent Part Number**	**QTY**	**Description**
	16557-69501	1	Exchange Board Assembly
A1	16557-66501	1	Board Assembly
A2	16555-61605	1	Cable Assembly (2x10)
A3	16710-61603	2	Cable Assembly-Logic Analyzer
A4	16555-61607	2	Cable Assembly-Internal Reference
A5	16555-61608	1	Cable Assembly-External Reference
A6	01650-61608	4	Probe Tip Assembly
A7	1252-4181	2	Probe Cable Socket - 50 pin
A8	16542-61607	1	Double Probe Adapter
A9	16555-68705	1	Cable Kit-Master/Expander (5 card)
E1	5959-9333	1	Probe Leads Replace (5 Per Package)
E2	5959-9334	4	Probe Ground Replace (5 Per Package)
E3	5959-9335	0	Pod Ground Replace (2 Per Package)
E4	5090-4356	4	Grabber Kit Assembly (20 Grabbers Per Package)
H1	16500-22401	2	Panel Screw
H2	16550-29101	1	Ground Spring
H3	0510-0684	2	Retaining Ring
H4	0515-0430	4	MS M3.0X0.5X6MM PH T10 (Endplate Screw)
H5	0515-2306	4	Screw Sems M3 X 0.5X10mm (Cable Retaining Screw)
MP1	01650-94312	1	Label-Probe and Cable
MP4	16550-40501	1	Module Panel
MP5	16555-07201	1	Module Panel Insert
MP6	16557-94301	1	Label-ID
MP7	7121-0850	4	Label-Antistatic
MP8	16555-60001	2	Ferrite Core Assembly

Exploded View



Exploded view of the 16557D logic analyzer

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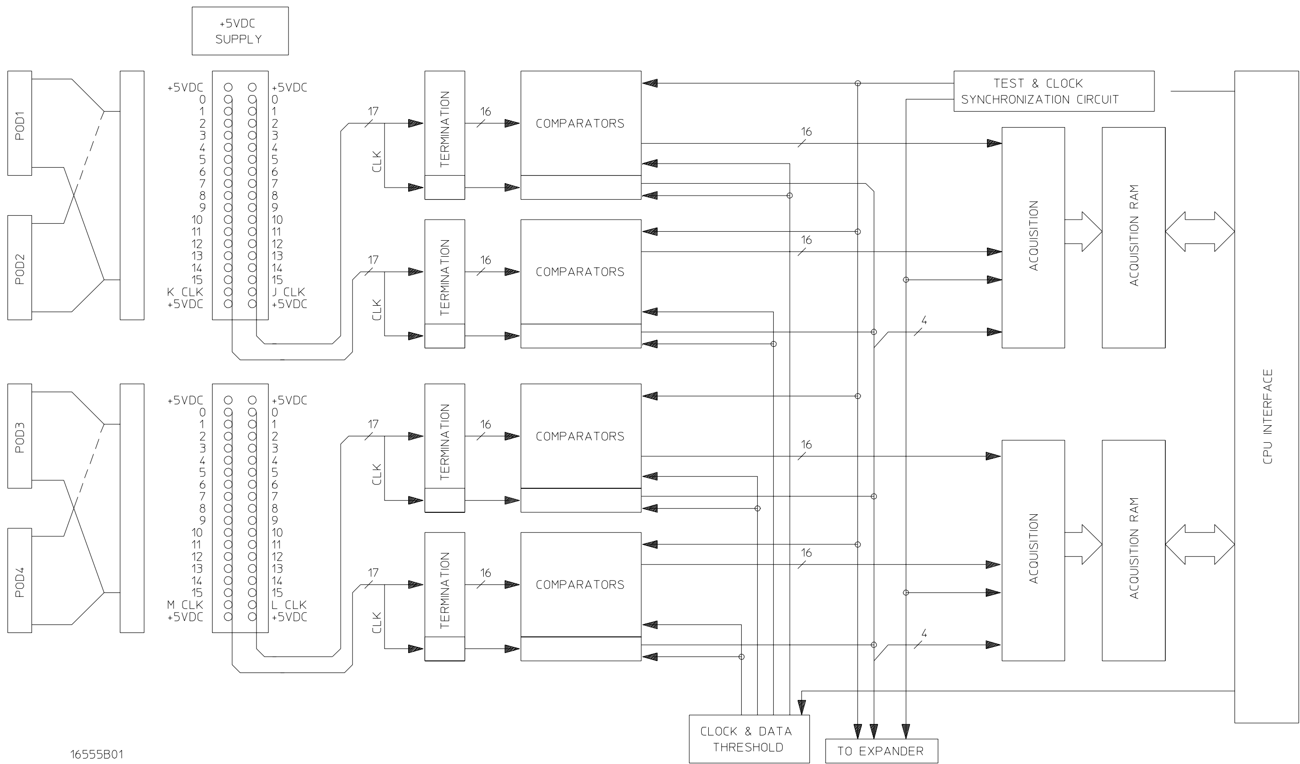
Theory of Operation

This chapter presents the theory of operation for the logic analyzer module and describes the self-tests. The information in this chapter is to help you understand how the module operates and what the self-tests are testing. This information is not intended for component-level repair.

Block-Level Theory

The block-level theory of operation is divided into two parts: theory for the logic analyzer used as a single-card module or as a master card in a multi-card module, and theory for the logic analyzer used as an expander card in a multi-card module. A block diagram is shown before each theory.

The 16557D logic analyzer



Probing. The probing system consists of a tip network, a probe cable, and terminations which reside on the analyzer card. Each probe cable is made up of two woven cables, each one carrying 16 data channels and 1 clock/data channel. The four clock/data channels on each logic analyzer plus the 64 data channels on each logic analyzer card results in a maximum of 68 available data acquisition channels for each card.

Each channel of the probing system has its own ground. In addition the pod has a single ground. For applications where many channels are used (greater than three) and signal risetimes are less than 3 ns, individual channel grounds should be used.

The probe tip networks comprise a series of resistors (250 Ohm) connected to a parallel combination of a 90 KΩ resistor and a 8.5 pF capacitor. The parallel 90 KΩ and 8.5 pF capacitor along with the lossy cable and terminations form a divide-by-ten probe system. The 250-Ohm tip resistor is used to buffer (or raise the impedance of) the 8.5 pF capacitor that is in series with the cable capacitance.

Comparators. Two 9-channel comparators interpret the incoming data and clock signals as either high or low, depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparators has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparators. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, the operating system software can test all data and clock channel pipelines on the circuit board through the comparator.

Acquisition. Each acquisition circuit is made up of a single acquisition IC. Each acquisition IC is a 34-channel state/timing logic analyzer. Two acquisition ICs are included on every logic analyzer card for a total of 64 data channels and 4 clock/data channels. All of the sequencing, storage qualification, pattern/range recognition and event counting functions are performed by the acquisition IC.

Also, the acquisition ICs perform master clocking functions. All four state acquisition clocks are sent to each acquisition IC, and the acquisition ICs generate their own sample clocks. Every time the user selects RUN, the acquisition ICs individually perform a clock optimization before data is stored.

Clock optimization involves using programmable delays in the acquisition ICs to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a four-phase 125-MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (125 MHz and faster), the four-phase 125-MHz clock signal determines the sample period. For slower sample rates, one of the two acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The sample clock is then sent to the other acquisition ICs.

Acquisition RAM. The acquisition RAM is external to the acquisition IC. The acquisition RAM consists of 18 RAM ICs (256K x 16). A memory management circuit controls RAM addressing during an acquisition run and during data upload to the mainframe CPU.

Test and Clock Synchronization Circuit. ECLinPS (ECL in pico seconds) ICs are used in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification (self-tests). The test patterns are propagated across all data and clock channels and read by the acquisition ICs to verify that the data and clock pipelines are operating correctly.

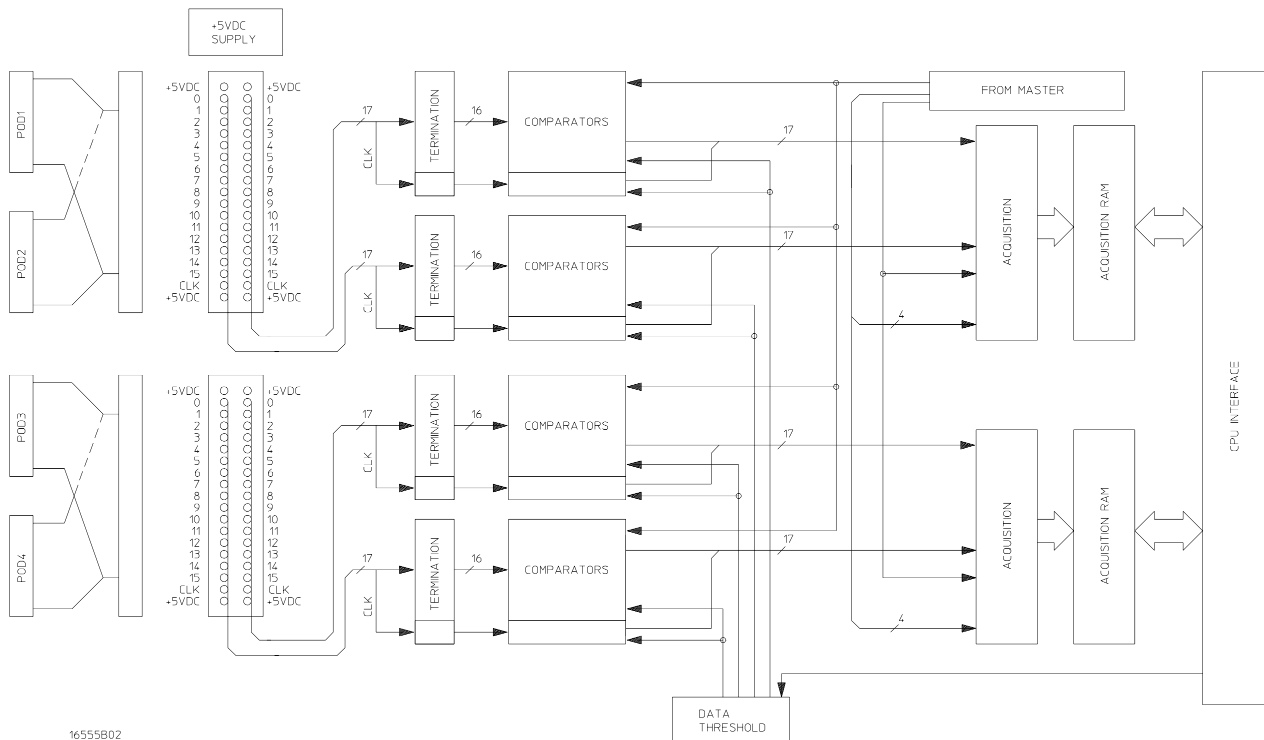
Also, the Test and Clock Synchronization Circuit generates a four-phase 125-MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. At fast sample rates, the synchronizing signal keeps the internal clocking of the individual acquisition ICs locked in step with the other acquisition ICs in the module. At slower sample rates, one of the acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The slow speed sample clock is then used by both acquisition ICs.

Clock and Data Threshold. The threshold circuit includes a precision octal DAC and precision op amp drivers. Each of the eight channels of the DAC is individually programmable which allows the user to set the thresholds of the individual pods. The 16 data channels and the clock/data channel of each pod are all set to the same threshold voltage.

CPU Interface. The CPU interface is a programmable logic device that converts the bus signals generated by the microprocessor on the mainframe CPU card into control signals for the logic analyzer card. All functions of the state and timing card can be controlled from the backplane of the mainframe system including storage qualification, sequencing, assigning clocks and qualifiers, RUN and STOP, and thresholds. Data transfer between the logic analyzer card and the mainframe CPU card is also accomplished through the CPU interface.

+5 VDC supply. The +5 VDC supply circuit supplies power to active logic analyzer accessories such as preprocessors. Thermistors on the +5 VDC supply lines and on the ground return line protect the logic analyzer and the active accessory from overcurrent conditions. When an overcurrent condition is sensed, the thermistors create an open that shuts off the current from the +5 VDC supply. After a reset time of approximately 1 minute, the thermistor closes the circuit and makes the supply current available.

The 16557D logic analyzer as an expander



The logic analyzers can be connected together in multi-card master/expander configuration. All of the functions of the logic analyzer configured as a master are retained by the logic analyzer configured as an expander with a few exceptions. As a master and expander multi-card logic analyzer module, most of the supporting circuitry on the expander configured card is disabled to allow both the master and expander cards to operate together as one module with no compromise in functionality in 136-channel, 204-channel, or 272-channel configurations. A 340-channel multi-card module is configurable with reduced specifications. Refer to chapter 1 for more information.

The same signals that drive the acquisition ICs on the master configured card also drive the acquisition ICs on the expander configured card.

Acquisition. The four clocks sent to the master card are also sent to the acquisition ICs on all expander cards. The acquisition ICs on the expander cards individually generate their own sample clock for the state acquisition mode. For timing acquisition mode, the master card also passes the synchronization signal to the expander cards.

The four clock/data lines on expander card pods are not available for either state mode clocking or state clock qualification. However, the four clock/data lines are still available as data channels.

Test and Clock Synchronization Circuit. The signals generated by the Test and Clock Synchronization Circuit of the master card are sent to all expander cards. Consequently, the Test and Clock Synchronization Circuit on each expander card is disabled to allow the master-configured card to drive the expander-configured card. The functionality of the Test and Clock Synchronization Circuit remains the same, but the circuit drives up to 8 more Acquisition IC and up to 16 more comparator test inputs.

Threshold. The thresholds of each of the expander card pods are individually programmable, as with the master card pods. The threshold of the data and clock/data channels of each pod is set to the same threshold voltage. The clock/data channel on each pod of the expander card is available only as a data channel.

Self-Tests Description

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

PLD Tests. Programmable Logic Devices (PLD) are utilized as an interface between the Agilent Technologies 16700-series Logic Analysis System backplane and the logic analyzer module. The PLD tests (Dpath Test and Accel Test) verify the operation of the data bus through the PLD. Test patterns are sent to the module and are written to a block of module memory. The patterns are then read and compared with known values. Also, a HW acceleration test verifies the PLD’s high-speed pattern search operation.

Passing the PLD Tests implies that the PLD is not corrupted and that data can be passed between the logic analyzer module and the backplane of the logic analysis system mainframe.

VRAM Tests. After verifying the integrity of the memory address bus, the acquisition RAM is checked by filling the RAM with a checkerboard pattern of "1s" and "0s," then reading each memory location and comparing the test pattern with known values. Then the RAM is filled with an inverse checkerboard pattern, read, and compared with known values. The acquisition ICs are then used to generate a walking "1s" pattern, which is stored in RAM. The patterns are then read and compared with known values.

Passing the memory test implies that the acquisition RAM is functioning and that each memory location bit can hold either a logic "1" or logic "0." Passing this test also implies that the RAM is addressable by both the acquisition ICs and the mainframe CPU system through the CPU interface.

Calibration Test. The Calibration test exercises the clock optimization circuit on-board the acquisition IC. The clock-optimization circuit optimizes the operation of the module. A test signal is generated by the comparators and sent to the acquisition IC. A test run is then done to see if the clock optimization circuit aligns the data signal with the master clock signal.

Passing the Calibration Test implies the clock optimization circuit that resides on the acquisition IC operates properly. Consequently the acquisition IC can properly sample data with minimal channel-to-channel skew.

Oscillator Test. The Oscillator Test functionally verifies the two oscillators and the oscillator internal pathways on the logic analyzer module. The oscillators are checked using the event counter on one of the acquisition ICs. The event counter will count the number of oscillator periods within a pre-determined time window. The count of oscillator periods is then compared with a known value.

Passing the Oscillator Test implies that both oscillators on the logic analyzer module are operating properly.

Comparator Test. The comparators in the logic analyzer front end are checked by varying the threshold voltage and reading the state of the activity indicators. The output of the comparator DAC is set to the upper voltage limit and the activity indicators for all the pod channels are read to see if they are all in a low state.

The DAC output is then set to the lower voltage limit, and the activity indicators are read to see if they are in a high state. The DAC output is then set to 0.0 V, allowing the comparators to recognize the test signal being routed to the test input pin of all of the comparators. Consequently, the activity indicators are read to see if they show activity on all channels of all the pods.

If the Comparator Test reveals that a logic analyzer channel is not recognizing the test data, a message will appear alerting the user that the channel is not operating as expected. If the module cannot be immediately serviced, then the user is alerted so that the failed channel will not be used until the module can be serviced.

Passing the Comparator Test implies that the logic analyzer front end is operating properly and all channels are capable of passing data to the acquisition ICs.

Communication Test. The communication test (Chip Comm Test) verifies that communications pipeline between the various subsystems of the IC are operating. Checkerboard patterns of "1s" and "0s" are routed to the address and data buses and to the read/write registers of each chip. After verifying the communications pipelines, the acquisition clock synchronization signals that are routed from IC to IC are checked. Finally, the IC master clock optimization path is checked and verified.

Passing the communication test implies that the communications pipelines running from subsystem to subsystem on the acquisition IC are functioning and that the clock optimization circuit on the IC is functioning. Also, passing this test implies that the acquisition clock synchronization signals are functioning and appear at the synchronization signal output pins of the acquisition IC.

Encoder Test. The encoder is tested and verified using a walking "1" and walking "0" pattern. The walking "1" and "0" is used to stimulate all of the encoder output pins which connect directly to the memory ICs. Additionally, the post store counter in each of the acquisition ICs is tested.

Passing the encoder test implies that the encoder is functioning and can properly route the acquired data to the acquisition memory. Also, passing this test implies that the post store counter on the acquisition ICs is functioning.

Resource Test. The pattern, range, edge, and glitch recognizers are tested and verified. First, an on-chip test register is verified for correct operation. Next, the pattern comparators are tested to ensure that each bit in the recognizer as well as the logic driver/receiver are operating. The edge and glitch pattern detectors are then verified in a similar manner. The range detectors are verified with their combinational logic to ensure that the in- and out-of-range conditions are recognized.

Passing the resource test implies that all of the pattern, range, edge, and glitch resources are operating and that an occurrence of the pattern, edge, or glitch of interest is recognized. Also, passing this test implies that the range recognizers will detect and report in- and out-of-range acquisition data to the sequencer or storage qualifier. The drivers and receivers at the recognizer input and output pins of the acquisition IC are also checked to be sure they are functioning.

Sequencer Test. The sequencer, the state machine that controls acquisition storage, is tested by first verifying that all of the sequencer registers are operating. After the registers are checked, the combinational logic of the storage qualification is verified. Then, both the occurrence counter and the sequencer level counter is checked.

Passing the sequencer test implies that all 12 available sequence levels are functioning and that all possible sequence level jumps can occur. Also, passing this test implies that user-defined ANDing and ORing of storage qualified data patterns will occur, and that the occurrence counter that appears at each sequence level is functioning.

Chip Clock Test. The sample clock generator on the acquisition ICs are tested by first checking the operation of the clock optimization circuit. The state acquisition clock paths are then checked to ensure that each state clock and clock qualifier are operating by themselves and in all possible clock and qualifier combinations. The timing acquisition optimization circuit is then operationally verified. Finally, the timing acquisition frequency divider (for slower timing sample rates) is checked.

Passing the chip clock test implies that each acquisition IC can generate its own master clock whether the clock is generated using a combination of external clocking signals (state mode) or internal sample clock signals (timing mode).

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Hazardous voltage symbol.

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